Series-Resonance BiCMOS VCO with Phase Noise of -138dBc/Hz at 1MHz offset from 10GHz and -190dBc/Hz FoM

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The phase noise of oscillators limits the modulation Error Vector Magnitude (EVM) in wireless communications and SNR in high-speed data converters. The issue is particularly critical in the wireless infrastructure for 5G and beyond, where base stations and backhaul transceivers need extremely low phase noise to support wide bandwidth and spectrally efficient modulation schemes at high carrier frequency. Given the supply voltage, the phase noise in LC oscillators is reduced by scaling down the inductance and increasing power consumption. However, the Q degradation with too small inductors sets a lower bound on phase noise [1][2]. To overcome this limit, oscillators evolved from a single core to multi-core, with N oscillators coupled to scale down phase noise by 10 log(N). The concept was originally introduced with two cores [1] and then extended to four [2]-[4] and eight cores [5], giving ideally a phase noise reduction of 3, 6 and 9dB respectively. Nevertheless, mismatches between oscillators impair phase noise and penalize the figure of merit (FoM) [3]. Moreover, with the number of cores which grows exponentially, the extension of the approach for further phase noise reduction is not practical.

A circuit topology which breaks the phase noise barrier of conventional oscillators is proposed in this paper. By exploiting the series resonance of a tank, an extremely low phase noise is demonstrated with a single-core oscillator. Realized in a 55nm-BiCMOS technology the series-resonance VCO proves -138dBc/Hz phase noise at 1MHz offset from 10GHz, with 1.2V supply and -190dBc/Hz FoM. The phase noise, 10dB lower than what demonstrated by silicon oscillators at

similar frequency, matches the performance of commercial products in III-V technologies for the wireless infrastructure, test equipment and military applications [6].

The conceptual advantage of a series-tank oscillator to reach ultra-low phase noise is demonstrated by a comparison with the popular parallel-tank oscillator in Fig. 1. In both cases, the supply voltage V_{cc} sets an upper bound on the tank voltage swing, V_{max}. The phase noise at offset $\Delta\omega$ from the oscillation frequency ω_o is given by the equation in the top side of Fig.1. Assuming the same noise factor for the active circuits, F, and the same LC-tank with quality factor Q, the phase noise of the two oscillators is determined by the active power dissipated on the resonators, P. The equivalent resistance at resonance of the series tank, R_S, is Q^2 times lower than that of the parallel tank, R_P. Therefore, assuming $V_{max}=\alpha V_{cc}$ in both oscillators (being α a proportionality constant), P_{series} is Q^2 times higher than $P_{parallel}$, leading to a phase noise of the series-tank oscillator which is $10\log Q^2$ lower than with the parallel-tank. This remarkable feature was observed also from a theoretical phase noise study in a four-stage ring oscillator [7] but not yet proved experimentally.

To exploit the potential for high spectral purity of the series resonator it is necessary to devise an active circuit suitable to drive it properly. The cross-coupled differential pair, commonly employed in parallel-tank oscillators, shows a negative conductance at the equilibrium point and current saturation at large signal. The series tank needs an active circuit with the dual functionality, i.e. negative resistance at the equilibrium point and voltage saturation at large signal. The conceptual schematic of the proposed circuit implementation is shown in Fig.2. The series tank must be connected to the emitters of Q_1-Q_2, where the circuit provides the V_x-I_x characteristic drawn on the right side. The batteries V_{os} represent a bias circuit which shifts down the base voltages such that Q_1-Q_2 operate away from saturation. Q_1-Q_2 work as a differential emitter follower, forcing V_X to be equal to -V*, the differential voltage at the collectors. At the equilibrium point (I_x=0), the same current flows through the load resistors R/2, V* is zero and the two diodes D_P-D_N are off. The

positive feedback established by cross-coupling Q_1-Q_2 determines a negative resistance at the emitters nearly equal to the differential load resistance, $dV_x/dI_x \approx -R$. Oscillations built-up if $|R|>Rs$ (R_s is the tank resistance at the series resonance). If $|I_x|$ grows, the differential voltage drop on the load resistors rises, in magnitude, until one diode turns on (D_P if $I_X>0$, D_N if $I_X<0$) saturating V* and hence V_x to $\pm V_D$ (the diode voltage drop) when $|I_x| > V_D/R$.

The final schematic of the series-resonance VCO with the negative resistance adapted for operation at 10GHz is reported in Fig. 3. To minimize the noise sources the bias currents for Q_1-Q_2 are sustained by inductors L_T and, instead of using resistors, the biasing voltages (V_{B1},V_{B2}) are applied through large but compact inductors L_{B1}, L_{B2} (implemented as multiturn spirals with a trace of narrow width). Diode-connected HBTs implement D_P,D_N. A small and low-Q inductor L_P (~60pH) feeds the supply voltage to Q_1-Q_2 and resonates at 10GHz with parasitic capacitances, leading to a resistive impedance at the collectors (R, drawn in grey). The series tank, implemented with L_S~0.9nH and C_S~280fF has Q~20. The differential voltage at the collectors of Q_1-Q_2, V*, is ideally a square wave with amplitude limited by D_N-D_P to V_D. The tank voltage follows V* with some attenuation, β, introduced by the coupling capacitors C_C and $C_{B\text{-}EQ}$, the equivalent capacitance at the base of Q_1-Q_2. The fundamental component of the voltage across the tank is relatively low, $V_{tank}=(4/\pi)\beta V_D$, but the voltage on the capacitor C_S is Q-times V_{tank} and reaches over 15V. Therefore, to avoid reliability issues C_S is implemented with four MOM capacitors and two thick-oxide A-MOS varactors in series, such that the maximum voltage on each capacitor is less than 3V. To have a sinusoidal current in the series tank with amplitude $I_{tank}=V_{tank}/R_S$ the DC bias current in each branch, I_B, is set by V_{B1} to 250mA. The minimum supply voltage is $V_D+V_{ce\text{-}sat}$ ($V_{ce\text{-}sat}$ is the minimum collector-to-emitter voltage of Q_1-Q_2 to operate in active region) thus V_{cc}=1.2V is used. A differential buffer (not shown) senses the oscillator signal at the collectors of Q_1-Q_2.

Fig. 4 plots the minimum and maximum phase noise measured in the tuning-range. The phase noise at 1MHz offset varies from -138dBc/Hz at 9.96GHz to -135.3dBc/Hz at 10.2GHz. Measurements are performed with a spectrum analyzer, and at low offset frequency (< ~100kHz) are slightly impaired by the random-walk noise of the oscillator in free-run. The variation of the spot phase noise at 1MHz offset across the tuning range is reported in the top plot in Fig.5. The FoM, in the same plot, ranges from -190dBc/Hz to -188dBc/Hz. The bottom plot shows the tuning characteristic. The oscillation frequency covers 9.96GHz to 10.9GHz with V_{tune} from 0V to 3.5V and maximum Kvco of 400MHz/V. The supply pushing (measured but not shown) is 53MHz/V.

Measured results are compared with low phase noise VCOs in the 10-20GHz range in Fig. 6. With an excellent FoM, the phase noise of the series-resonance VCO is 10.1dB lower than [4] (a 4-cores VCO with V_{cc}=3V) and matches the performance of commercial products in III-V technology with less than half power dissipation [6]. The chip photo is shown in Fig. 7.

References

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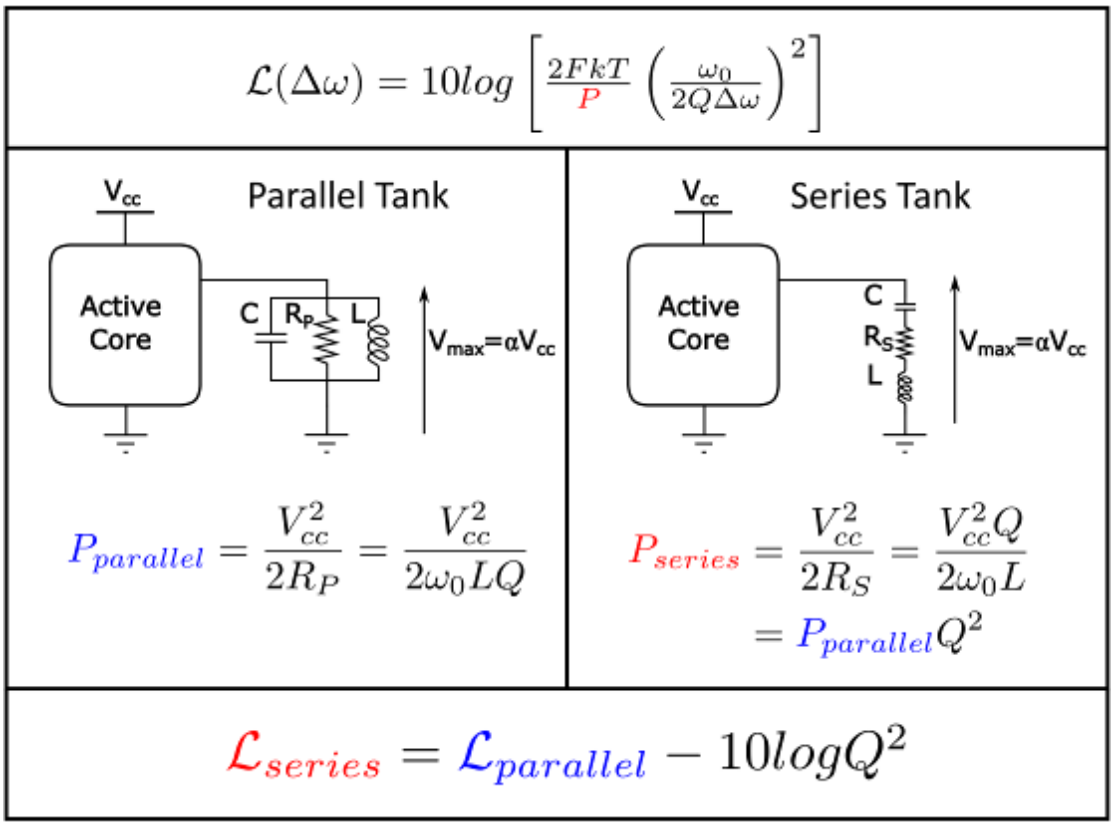


Figure 1: Phase noise comparison of parallel-tank and series-tank oscillators

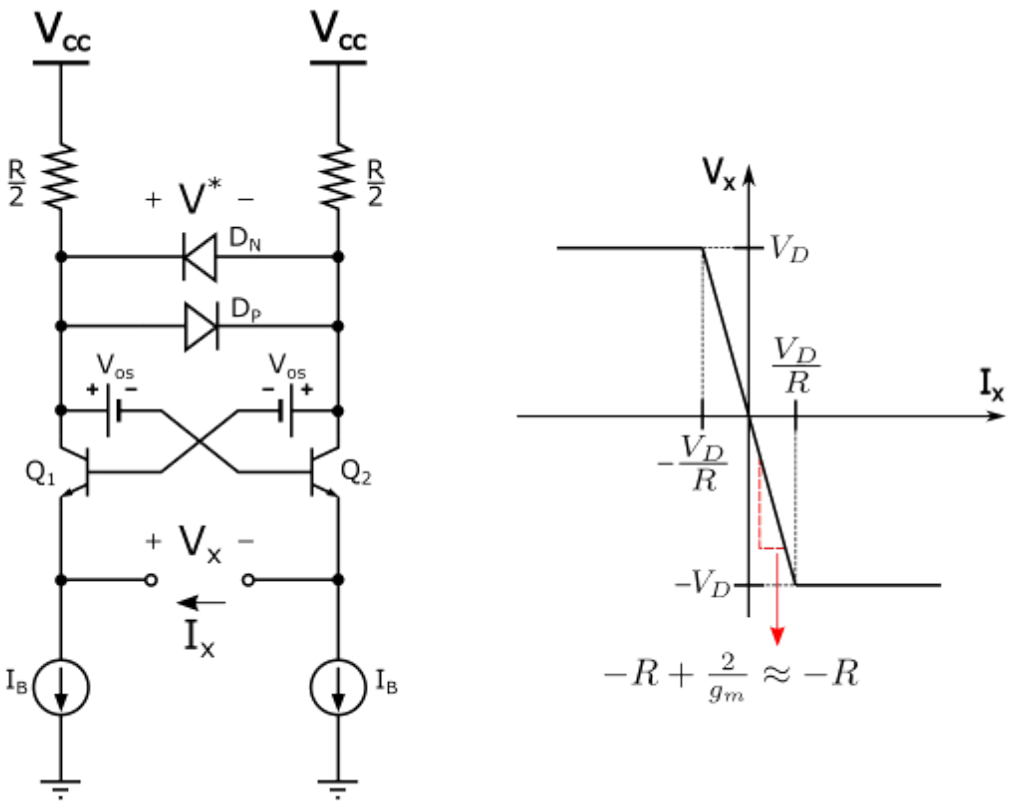


Figure 2: Negative resistance suitable to drive a series-tank oscillator

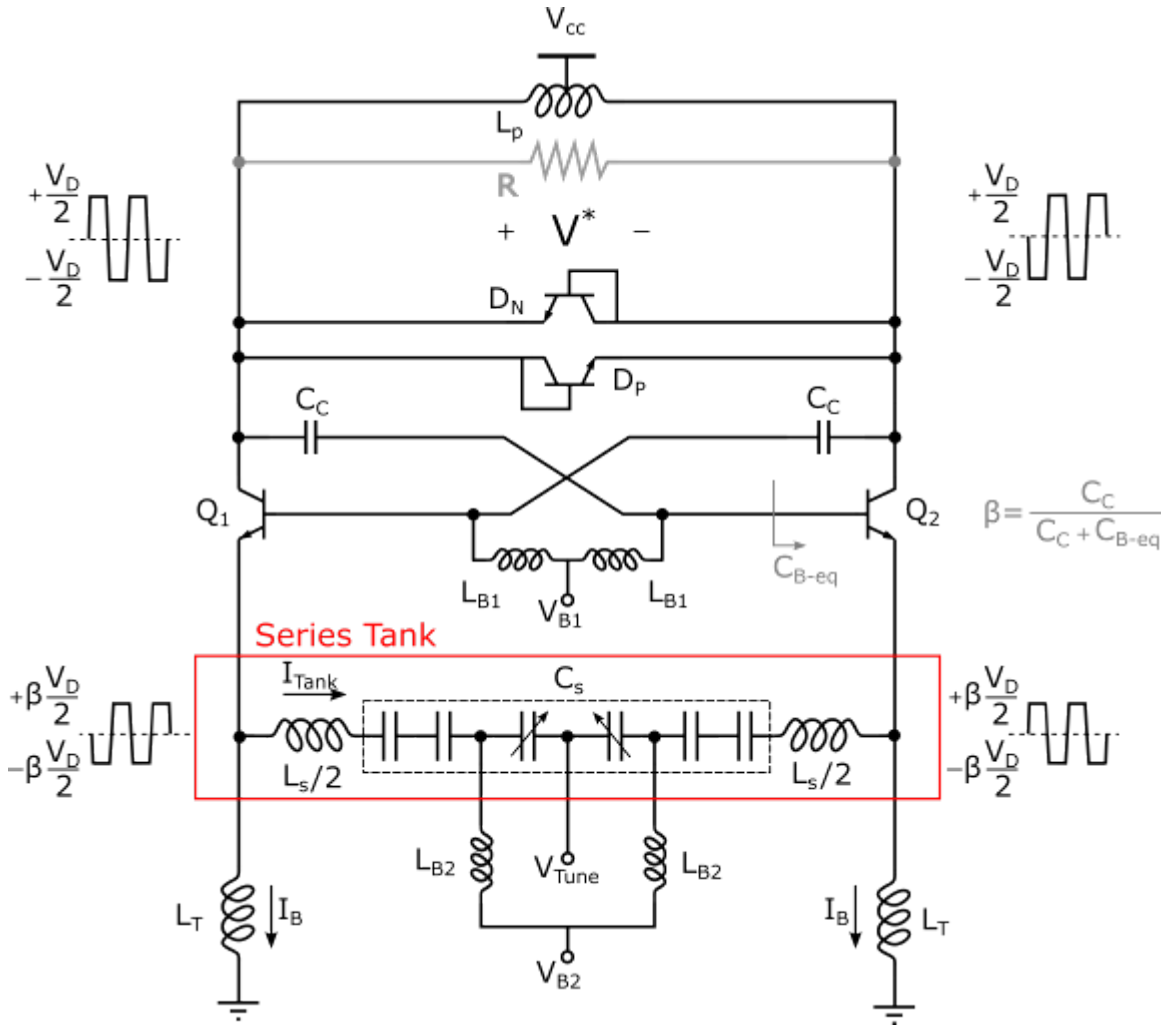


Figure 3: Schematic of the 10GHz series-resonance VCO.

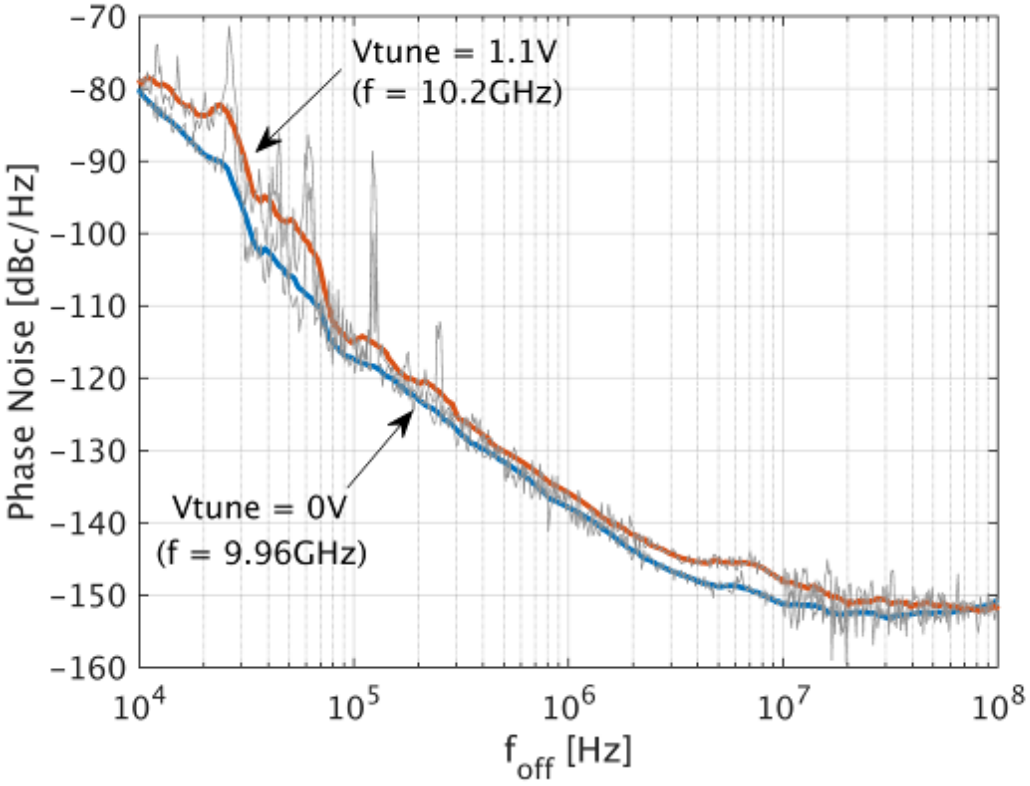


Figure 4: Minimum and maximum measured phase noise.

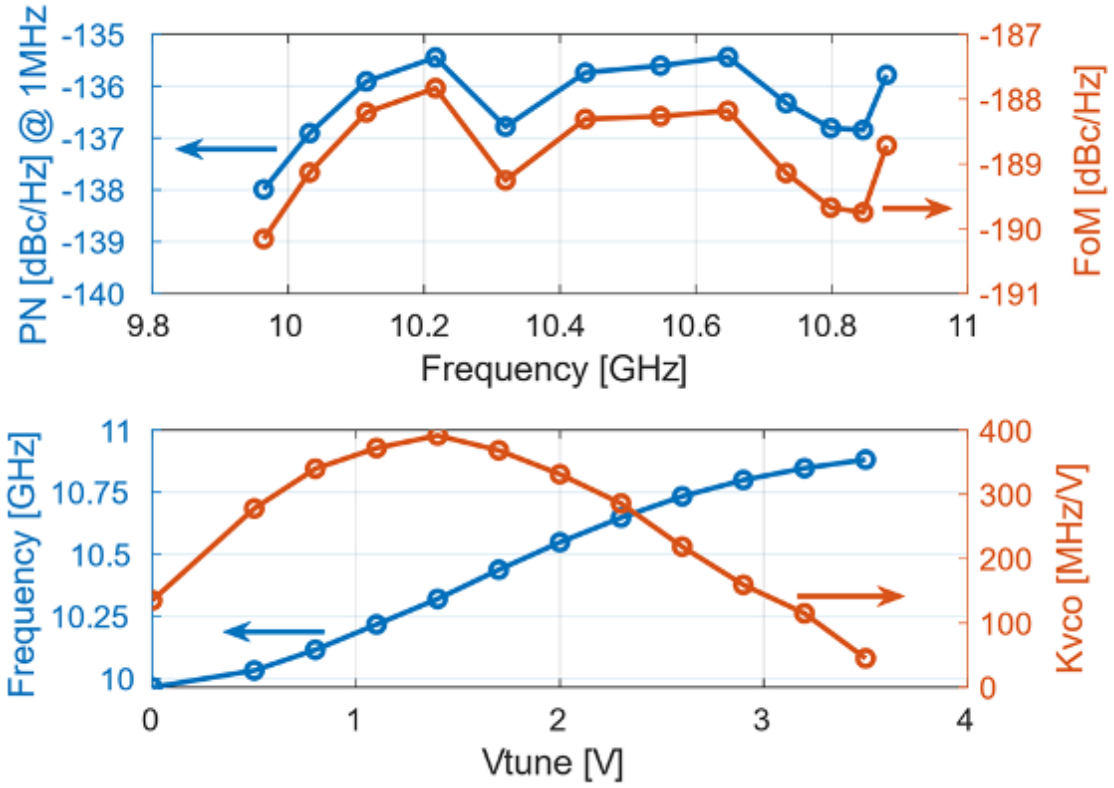


Figure 5: Phase noise at 1MHz and FoM versus oscillation frequency (top) and tuning characteristic (bottom)

Reference	Tech.	N.Cores	V_{DD} [V]	P_{DC} [mW]	f_0 [GHz]	TR [%]	Eq. PN(1MHz) @10GHz [dBc/Hz]	FoM [dBc/Hz]
MTT-IMS 2016	130nm BiCMOS*	1	2	58	19.8	9.8	120.3	-181
RFIC 2019	130nm BiCMOS	1	3.3	122	20	18	-125.9	-185
BCTM 2017	55nm BiCMOS	1	2.5	56	20.5	19	-125	-187.5
ESSCIRC 2017	130nm BiCMOS	1	4	70	21	20.5	-125.4	-187
RFIC 2018	120nm BiCMOS *	1	2.5	75	10.6	21.7	-123.9	-184
BCTM 2012	250nm SiGe:C	1	3.7	93	12.8	5	-125.5	-185
BCICTS 2019	130nm BiCMOS	1	3.3	45	17	15	-121	-184
JSSC 2018 [3]	55nm BiCMOS*	4	1.2	50	20	15	-124.5	-187.5
ISSCC 2018 [4]	130nm BiCMOS	4	3	72	15	16	-127.9	-189
RFIC 2021 [5]	28nm CMOS	8	1.1	173	10.7	27	-126.6	-184
Analog Devices HMC512 [6]	GaAs InGaP HBT	NA	5	1650**	10	11.7	-135	NA
This Work	**55nm BiCMOS**	**1**	**1.2**	**600**	**10**	**9**	**-138**	**-190**

*only CMOS used in VCO core
** including output buffer

Figure 6: Performance summary and comparison

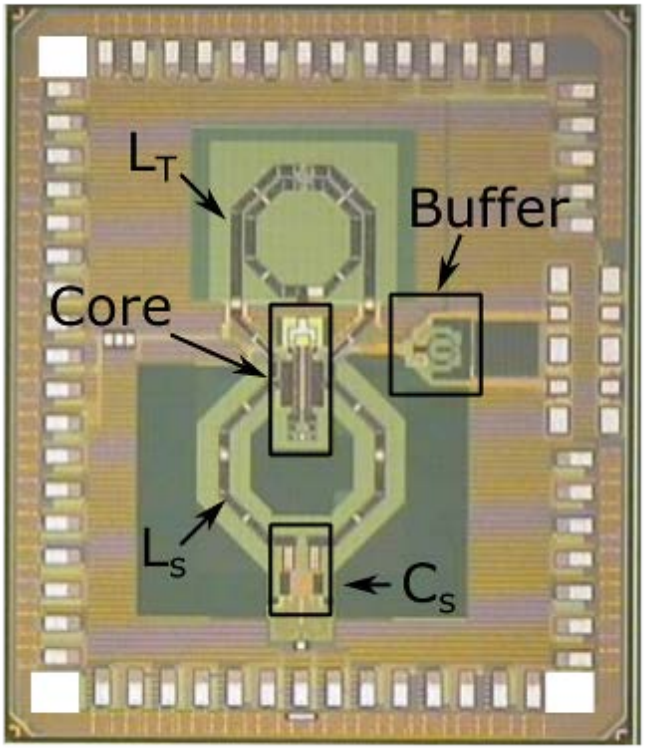
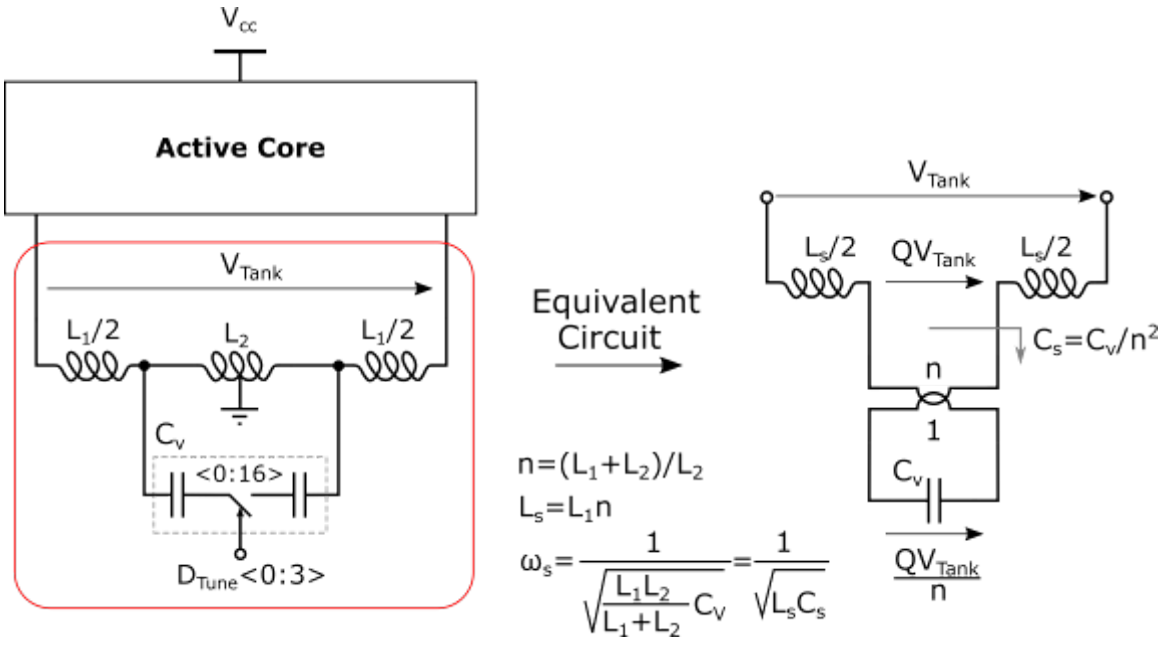
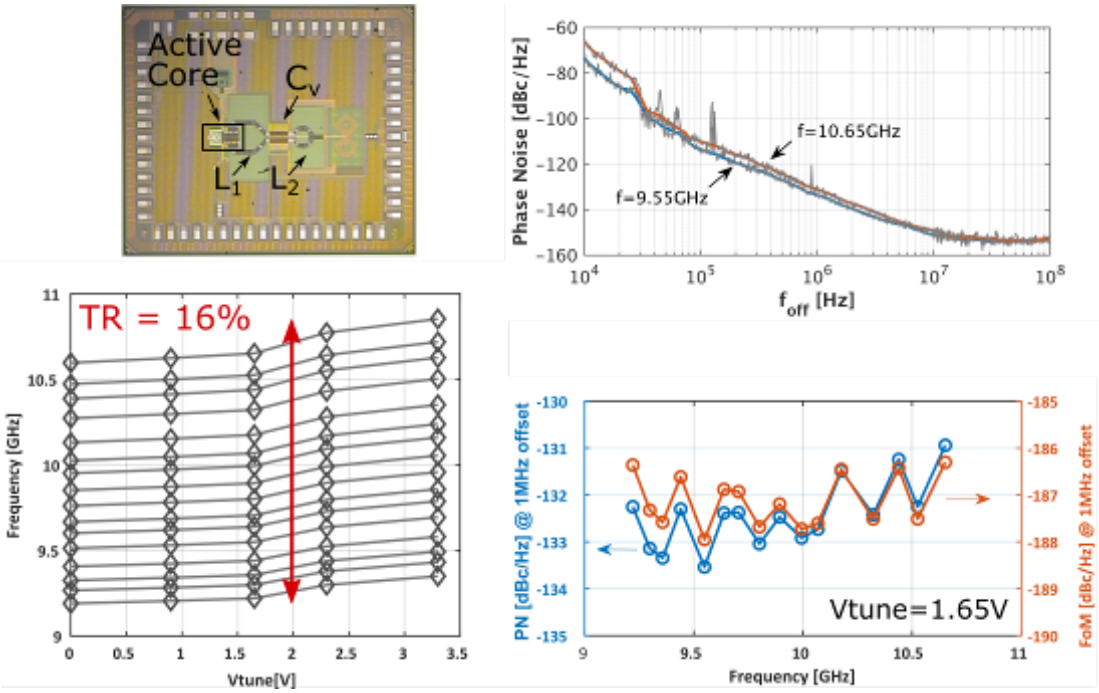


Figure 7: Chip photograph

Supplementary Material



S1. A second chip version of the oscillator has been realized with a resonator arrangement that limits the voltage swing on the capacitor thus not requiring multiple capacitors in series.
As shown on the left, the variable capacitor, (C_V, implemented here as a bank of digitally switched MOMs) shunts a fraction of the inductor (L_2). It can be proved that the L_1-L_2-C_V network is equivalent to a series resonator (right) where the capacitor is coupled with a *n:1* transformer ($n=(L_1+L_2)/L_2$). In this way, the voltage on the physical capacitor is reduced from QV_{Tank} to QV_{Tank}/n.



S2. Chip photo and measurements of the second version of the series-resonance VCO. This VCO is digitally tunable with 16% frequency variation around 10GHz. With 330mA from 1V supply, the phase noise at 1MHz offset ranges from -131 dBc/Hz to -133.5 dBc/Hz. The FoM ranges from -186.2dBc/Hz to -188dBc/Hz.