E-band Frequency Sextupler with >35dB Harmonics Rejection over 20GHz Bandwidth in 55nm BiCMOS

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***Abstract*— A frequency multiplier by 6 (sextupler) for LO generation in E-band is presented. It comprises a tripler, a doubler, and an output buffer. A detailed analysis is proposed to discuss the optimal order of the multiplication stages to minimize unwanted harmonics of the input. Moreover, novel circuit topologies for the tripler and doubler are introduced. The tripler core is devised to reproduce the trans-characteristic of a 3rd order polynomial that ideally generates only the 3rd harmonic of a sinusoidal input signal. By leveraging an envelope detector for adaptive biasing, the circuit maintains excellent suppression of the driving signal and unwanted harmonics over wide variations of the input power. The proposed topology improves output signal purity and current conversion efficiency against classical triplers based on transistors biased in class C. The cascaded frequency doubler is based on a novel push-push configuration that provides a differential output and excellent odd-order harmonic rejection thanks to an enhanced robustness to amplitude and phase unbalances of the driving signal. The sextupler is fabricated in a 55nm SiGe-BiCMOS technology. Driven with a 0dBm input signal and consuming 63.1mW of DC power, it delivers P_{out} up to 5.6dBm at 72GHz. P_{out} is above 0dBm over 20GHz bandwidth while undesired harmonics of the input are suppressed by more than 35dB. Compared to previously reported millimeter-wave frequency multipliers, the sextupler demonstrates improved harmonic rejection, conversion gain and efficiency, without compromising the operation bandwidth and output power.**

***Index Terms*—Frequency multiplier, sextupler, tripler, doubler, LO generation, BiCMOS, millimeter-waves.**

I. INTRODUCTION

Communications at millimeter waves (mm-waves) are rapidly gaining interest due to the wide available bandwidth which translates into higher data transmission capacity [1]. Generation of the transceivers local oscillation (LO) is critical because many contrasting requirements, i.e. tuning range (TR), phase noise (PN), output power, and level of spurious tones, affect the system performance. Differently from what is commonly pursued at radio frequency, LO generation with a phase locked loop (PLL) embedding a voltage-controlled oscillator (VCO) at the desired output frequency is not viable at mm-waves. In fact, the severe impact of device parasitics and the low quality factor of passive components in silicon (mostly variable capacitors) impair the achievable PN and TR. At mm-waves, designs in CMOS technology have reported around 10% of TR [2-4], while bipolar transistor technologies enable larger TR [5, 6], up to 28% in [7] using a BiCMOS process. However, in any case, digital frequency dividers in the PLL running at mm-waves need excessive power consumption.

A commonly pursued approach consists of a PLL in the 10-20GHz range, where silicon VCOs feature the best figure of merit, followed by a frequency multiplier. However, the multiplier must provide good suppression of the driving signal and undesired harmonics not to impair the transceiver performance, particularly with high-order, spectrally efficient modulation schemes [8].

LO generation at mm-waves or sub-THz range with a source at 10-20GHz requires a high multiplication factor. Sub-harmonic injection locked oscillators (S-ILO) suffer from narrow bandwidth due to the limited locking range (LR). In [9], a S-ILO multiplier by 13 to 15 with 12% fractional bandwidth output frequency was demonstrated implementing a frequency tracking loop for tuning the locked oscillator at 30GHz. The operation bandwidth is therefore limited by the frequency tuning range of the oscillator which is significantly penalized if the operation frequency is increased. N-push technique [10, 11], mixing [12-14], and edge combining [15] are other methods that can potentially allow high multiplication factors. They all rely on manipulation of equally spaced phase-shifted signals, with the accuracy of the phase shifts being crucial to achieve high spur rejection. The high output power and high spur rejection in [10] was achieved at the cost of a very small operation bandwidth (1.4%) and high power consumption of the multi-phase ring oscillator. The tripler architecture in [7], very well suited for advanced CMOS nodes, would be much less power efficient if implemented in a pure bipolar or BiCMOS technology. In addition, higher multiplication factor needs increasing the number of phases and if they are generated by a ring oscillator, increasing the number of stages reduces the oscillation frequency

A more robust approach is by cascading multiplication stages, of smaller factors, where harmonics of the input signal are generated by transistors biased in class B/C. Following this approach, a sextupler was proposed in [16], multipliers by nine in [17] and [18], and octuplers in [19] and [20], with respective rejection of unwanted harmonics of 25, 31, 37, 40 and 20 dB. Despite the medium to high achieved bandwidth in these works, the use of low-efficiency harmonic generation circuits and the need for several filtering stages to reach acceptable rejection of

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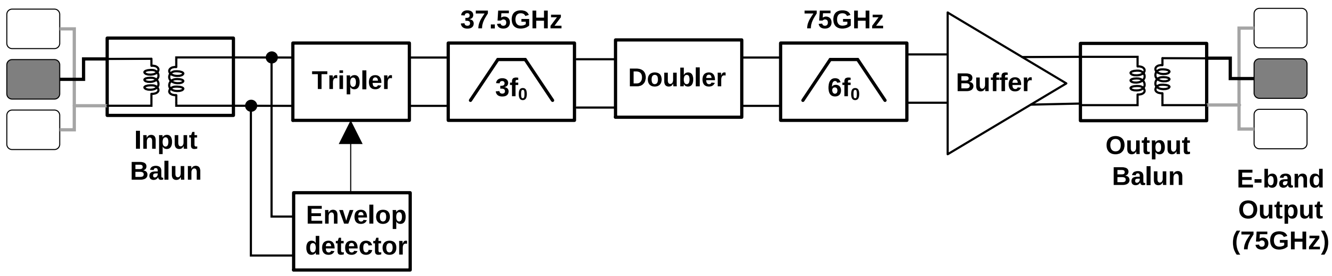


Fig. 1. Block diagram of the frequency multiplier by 6 (sextupler).

unwanted harmonics led to excessive power consumption, above 400mW, or very low output power. Combining class-C transistors with the high gain and high selectivity of ILO buffers improves the rejection of unwanted harmonics at low power consumption, as proved by the sextupler in [21] or the quadrupler in [22], but at the cost of respectively 1.5% and 6.9% fractional bandwidth only. Finally, mixing and injection locking techniques were used together in more sophisticated designs to cover a larger frequency range. In [23] the multiplication factor can be varied by programming switchable inductors, hence changing the number of harmonic to be locked on. However, application of the technique to higher frequency is challenging as inductors size shrink. Also in [24] and [25] different multiplication factors are available, but at different output taps, limiting its usage.

Comparison of the different methods to implement frequency multipliers with high multiplication factors reveals that cascaded stages excel at simplicity and robustness, hence they are preferrable at mm-waves frequency. On the other hand, the generation of several undesired harmonic components by transistors in class B/C sets a severe trade-off between the level of harmonics, operation bandwidth and power consumption. Meanwhile, sensitivities to transistor bias point or input power level appear as challenges to these otherwise robust circuits.

In this work, a frequency sextupler for LO generation at E-band with high harmonics rejection, wide bandwidth and low power consumption is proposed. Choice of the LO multiplication factor is driven by several aspects which includes location of spurious tones, availability or feasibility of the PLL, distribution of the signal and optimization of the overall power efficiency. The proposed sextupler is designed within the framework of the European project DRAGON, aimed at developing an high-capacity transceivers for backhaul in 5G and beyond [26], which makes use of a low phase noise commercial synthesizer in X band and needs generation of a signal in E-band. The block diagram of the sextupler is shown in Fig. 1. It is composed of a novel frequency tripler and doubler. The proposed tripler substantially improves the rejection of unwanted harmonics against class-C multipliers without relying on complex filtering stages [27]. A novel topology for the frequency doubler is also introduced. Compared to the widespread push-push doublers [28-30] the presented solution provides a differential output and excellent odd-order harmonic rejection thanks to an enhanced robustness to amplitude and phase unbalances of the driving signal. The sextupler is realized in a 55nm SiGe-BiCMOS technology. A test chip consumes 63.1mW of DC power of which 39.1mW is consumed by the output buffer. The maximum output power is 5.6 dBm and remains above 0dBm from 64.7 GHz to 84.7 GHz, while all undesired harmonics are suppressed by at least 35 dB.

The rest of the paper is organized as follows: Sec-II analyzes the challenges of the most widely adopted solutions for harmonic generation in mm-waves frequency multipliers. Sec-III describes the proposed sextupler architecture with a discussion about the most convenient ordering of multiplier stages to minimize the level of unwanted harmonics. The proposed tripler is introduced in Sec. IV while the doubler and output buffer are presented in Sec-V. Measurements are reported in Sec. VI where the results are also compared with previously reported mm-waves frequency multipliers. Sec. VII concludes the paper.

II. Frequency Multiplication with Class-B/C Transistors

The most common approach for frequency multiplication is by generating harmonics of a driving signal with a transistor biased in class-B/C, as shown in Fig. 2a, and selecting the desired harmonic with a frequency selective load impedance. For frequency multiplication by N, the LC load is tuned to a center frequency of Nf_0 (being f_0 the input signal frequency). The -3dB bandwidth (BW) is inversely proportional to the filter quality factor: $BW = Nf_0/Q$. The harmonic content of the transistor current, I_{out}, is set by the transistor conduction angle, θ, determined by the bias voltage V_{bias}. To gain insight, the top plot in Fig. 2b reports the simulated short-circuit collector currents at fundamental frequency, 2nd, and 3rd harmonic (I_{f0}, I_{2f0}, I_{3f0} respectively), normalized to transistor area, as a function of the estimated θ. The harmonic rejection ratio (HRR), defined as the ratio between the power of the desired signal and the power of unwanted harmonics, is limited by I_{f0}, i.e. the leakage of the driving signal, which is always larger than $I_{2f0,3f0}$, as evident also from the bottom plot in Fig. 2b, showing the ratio I_{f0}/I_{2f0} and I_{f0}/I_{3f0}. The optimum conduction angle for the desired harmonic can be selected based on the required HRR and output power. As an example, in case of a tripler, θ≈140° maximizes I_{3f0} and hence the tripler output amplitude but I_{f0} is 10dB larger than I_{3f0} (bottom plot). Targeting a bandwidth of 15% (Q=6.7) the rejection of I_{f0} from the LC load is 20log(3)+20log(Q)=26dB, leading to HRR=26-10=16dB only on the tripler output voltage (V_{out}). Looking at the plots in Fig.

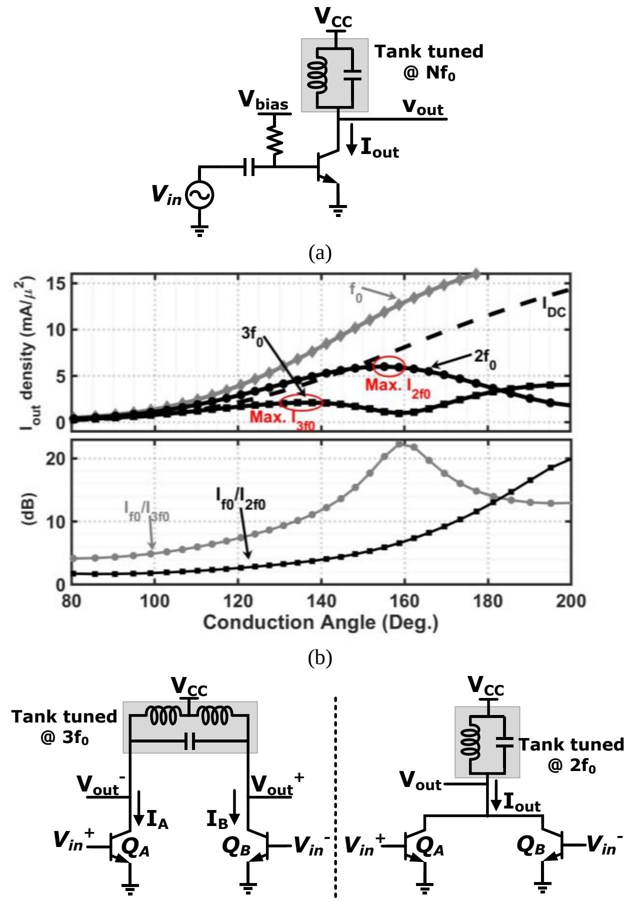


Fig. 2. (a) Single BJT biased in class-B/C as a harmonic generator, (b) Harmonics of I_{out}, (c) Differential version for odd-order multipliers, (d) Differential version for even-order multipliers (push-push).

2b, I_{f0}/I_{3f0} is minimized (from 10dB to 4dB) at low θ. This improves HRR by 6dB, from 16dB to 22dB. However, I_{3f0} at θ≈80° is roughly 7 times lower than at θ≈140°. Therefore, the mild improvement of HRR comes at the price of 17dB output amplitude reduction. A similar conclusion can be drawn for the case of a doubler. That is, HRR can be mildly improved at the price of significant reduction of the desired tone's amplitude. In addition, limited current conversion efficiency, $\eta_C = I_{Nf0}/I_{DC}$, (being N the number of the desired harmonic) is another limitation of harmonic generation with class-B/C transistors. Looking at the curves in Fig. 2b and considering the case of a tripler, we can see that η_C is at most 0.5 at the angle of maximum I_{3f0}.

In summary, despite its simplicity, the class-B/C multiplier suffers from poor suppression of the driving signal and efficiency. As shown in Fig. 2c and Fig. 2d, the performance of class-B/C harmonic generators can be improved to realize multipliers by odd or even factor respectively. In a differential topology (Fig. 2c) the odd harmonics of the input signal in I_A and I_B are in opposite phase, following $V_{in}^{\pm}$, whereas the even harmonics are in phase. Therefore, the even harmonics of the input are ideally canceled on the differential output. Nevertheless, the strong leakage of the driving signal is not cancelled.

Frequency triplers based on topologies depicted in Fig. 2a and Fig.2c are widely reported in the literature. The HRR, dominated by leakage of the driving signal, is typically in the 20-30dB range [31-35]. The suppression of the driving signal could be improved by rising the filter selectivity at the cost of larger power consumption or bandwidth limitation [36].

The circuit topology in Fig.2d, (commonly named push-push) is employed in frequency doublers. The anti-phase odd harmonics of the differential input signal cancel each other while the even harmonics add constructively. Ideally, there should be no fundamental component introduced by a balanced doubler. However, the fundamental tone is always present due to device mismatches, amplitude and phase unbalances in the input signals and capacitive coupling. As a matter of fact, the leakage of the driving signal remains the dominant spurious tone, still limiting the HRR to 20-30dB. Many works have demonstrated use of the push-push stage [28-30, 37, 38] or alternative topologies [39] at various frequencies and achieved wide bandwidth with around 20dB suppression of the driving signal. In [40] the leakage of the fundamental has been associated in part with the imbalances of the input balun, hence with a careful design focused to improve symmetry of the balun, 30dB suppression of the f_0 was achieved.

III. Frequency Sextupler Architecture

The proposed frequency sextupler, already introduced in Fig. 1, is composed of a tripler, a doubler, and an output buffer. When frequency multipliers are cascaded, intermodulation of each stage folds the harmonics generated by the previous stage and creates new harmonic tones at the output. As an example, if a tripler precedes a doubler, the component at f_0 leaked to the tripler output can get mixed with the main component at $3f_0$ and generate a tone at $4f_0$ at the doubler output. This issue is critical as tones generated by intermodulation can be very close to the desired signal and finally difficult to be filtered out. Therefore, an important aspect to be considered is the order of the multiplication stages that keeps the spurious tones from intermodulation low and as far as possible from the main tone. In case of a frequency sextupler, there are two options: *Tripler first* and *Doubler first*.

As discussed in the previous section, the largest undesired output tone in both doublers and triplers is the leakage of the driving signal. Therefore, assuming a sinusoidal input, $x(t) = A\cos(2\pi f_0 t)$, the operation of a frequency doubler can be approximated by the following polynomial:

$$y(t) = \frac{1}{A\,\rho}\,x(t) + \frac{2}{A^2}x(t)^2 \quad (1)$$

where ρ accounts for the finite doubler suppression of the tone at f_0 with respect to $2f_0$ i.e. $\rho = y_{2f_0}/y_{f_0}$ (y_{2f_0}, y_{f_0} are the fundamental and second harmonic of y) Similarly, the tripler operation can be approximated by the following polynomial:

$$w(t) = \frac{1-3\gamma}{A\,\gamma}\,x(t) + \frac{4}{A^3}x(t)^3 \quad (2)$$

where γ accounts for the tripler suppression of the tone at f_0 with respect to $3f_0$ i.e. $\gamma = w_{3f_0}/w_{f_0}$ (w_{3f_0}, w_{f_0} are the fundamental and third harmonic of w)

Modeling the doubler and the tripler with (2) and (3), the two options for implementing a sextupler can now be compared.

A. *Doubler First:*

When the doubler is the first block in the chain, using (1) and omitting the generated DC component, the output is:

$$y(t) = \frac{1}{\rho}\cos(\omega_0 t) + \cos(2\omega_0 t) \quad (3)$$

The doubler output is then fed to the tripler. By substituting (3) in (2) and keeping only the tones closest to the desired one $(6\omega_0 t)$, the sextupler output is approximated by:

$$w(t) \approx \frac{3}{\rho^2}\cos(4\omega_0 t) + \frac{3}{\rho}\cos(5\omega_0 t) + \cos(6\omega_0 t) \quad (4)$$

As the 5th harmonic is the closest tone to the desired $6\omega_0$ signal (thus it is the most difficult to filter out) we focus our attention to it. Assuming $\rho = 30$, which corresponds to 29.5dB of driving signal suppression of the doubler alone, consistent with the results in the literature [33-35], from (4) the 5th harmonic is only 20dB below the desired signal.

B. *Tripler first:*

Following the same approach as in the previous case, using (2) the output of a tripler excited by a single tone at ω_0 can be approximated by

$$y(t) = \frac{1}{\gamma}\cos(\omega_0 t) + \cos(3\omega_0 t) \quad (5)$$

The tripler output is then fed to a doubler. In this case, the doubler output is obtained by substituting (5) in (1). Keeping only the tones closest to $6\omega_0$, the output is:

$$w(t) \approx \frac{2}{\gamma}\cos(4\omega_0 t) + 0 \times \cos(5\omega_0 t) + \cos(6\omega_0 t) \quad (6)$$

Comparing (6) and (4) leads us to an important result: in the case of *tripler first,* the 5th harmonic ideally disappears. This is a key difference because, due to the small spectral distance to the desired tone, filtering the 5th harmonic is challenging.

In the above analysis, made by approximating the two multipliers with (1) and (2), only the finite suppression of the driving signal frequency has been considered. A more accurate analysis can be done by considering more terms in the polynomials responsible for leakage also of the 4th harmonic in the doubler and 5th harmonic in the tripler. The 4th and 5th harmonics are assumed 10dB lower than the leakage of the fundamental, a realistic scenario assuming that the two circuits are cascaded with mild interstage filtering. Fig. 3 shows a graphical representation of the results assuming ρ=γ=30. The 4th and 8th harmonics at the output of the sextupler ($4f_0$, $8f_0$) are almost equally suppressed in both cases. However, the *tripler first* chain (Fig. 3b) provides 48dB more suppression of the 5th harmonic and the 7th harmonic ideally disappears completely[1]. The more accurate analysis confirms that placing the tripler before the doubler is still preferrable to limit the level of undesired harmonics at the output.

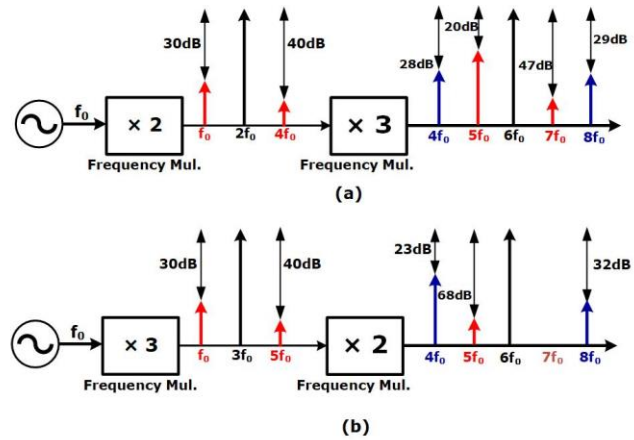


Fig. 3. Effect of multipliers' order on output spurs. (a) *Doubler first*, (b) *Tripler first*.

Another important observation that can be made with the above analysis is the influence of harmonic rejection levels of the first and second block in the chain on the overall harmonic rejection. By assigning different values to γ and ρ in the two cases considered, it is observed that the first block plays always a more dominant role. As an example, in the case of *tripler first*, $\gamma = 20$ and $\rho = 40$ results in 19.6 dB and 29 dB suppression of the 4th and 8th harmonics, respectively, whereas $\gamma = 40$ and $\rho = 20$ results in 25.6 dB and 34.5dB suppressions. Therefore, it can be concluded that particular care must be paid on the harmonic suppression performance of the first stage to maintain low level of unwanted harmonics at the output of the chain.

IV. FREQUENCY TRIPLER

A. *Principle of operation*

Assuming a sinusoidal driving voltage, $V_{in}(t)=A\sin(2\pi f_0 t)$, the active core of an ideal tripler that generates current only at the 3rd harmonic must display a trans-characteristic which follows the 3rd order polynomial[2]:

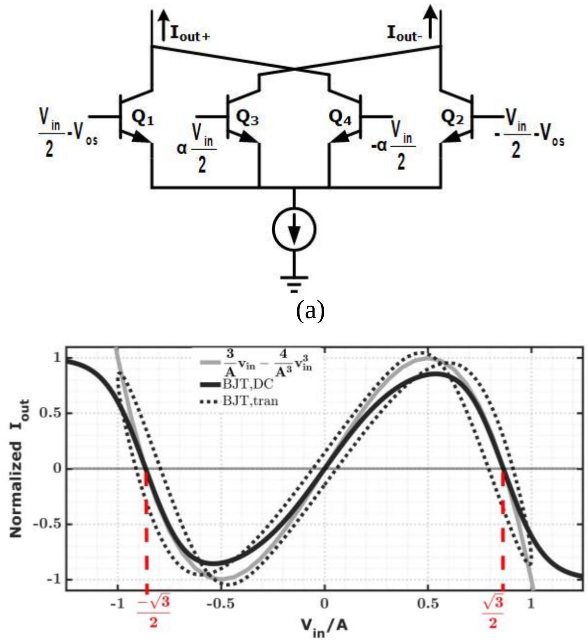
$$I_{out} = \left(\frac{3}{A}v_{in} - \frac{4}{A^3}v_{in}^3\right)g_m \quad (7)$$

Fig. 4a shows the proposed circuit schematic to approximate (7) while the ideal and transistors trans-characteristics are plotted in Fig. 4b.

Looking at the circuit schematic, $Q_{3,4}$ are driven by the input signal attenuated by α while $Q_{1,2}$ are directly driven by the input signal but with a negative DC level shift ($-V_{os}$) with respect to the base of $Q_{3,4}$. The circuit operation is as follows: at small V_{in}, the lower bias voltage keeps $Q_{1,2}$ off and the circuit approximates (7) near the origin with a simple differential pair formed by $Q_{3,4}$. But when V_{in} rises, $Q_{1,2}$ turn on, subtract current from the outputs and reverse the slope of the trans-characteristic. Notably, at each half cycle almost all the tail current is steered to one branch and then to the other, creating a

[1] This is true under the assumption that the tripler is fully balanced and no even harmonic is present at its output. However, if the tripler generates also the 4th harmonic, it will be mixed with the 3rd one and a tone at the 7th harmonic will be generated at the doubler output. Therefore, this tone normally does not totally vanish in practical cases.

[2] The presence of A in Eq.(7) means that the trans-characteristic has to be adapted to the amplitude of the input signal.



(b)

Fig. 4. (a) Simplified schematics of the proposed tripler core (b) comparison of the trans-characteristic with Eq. (7).

3rd harmonic current at the output with an amplitude close to that of the tail DC current. This implies a current conversion efficiency close to one. Looking at the upper plot in Fig. 2b, in a multiplier based on the non-linearity of a transistor biased in class-C, the magnitude of I_{3f0} is close to half of I_{DC} at maximum I_{3f0}, implying a current conversion efficiency roughly half of the proposed circuit.

The zero crossings of the current offsetted from the origin in the trans-characteristic of Fig. 4b occur when the voltage at the base of $Q_{3,4}$ equals the voltage at the base of $Q_{1,2}$ i.e. $½\alpha V_{in}=½V_{in}-V_{os}$. This condition is satisfied for $V_{in} = \pm 2V_{os}/(1-\alpha)$. The zero crossings of (7) are at $V_{in} = \pm\sqrt{3}A/2$. Therefore, V_{os} and α must be selected to satisfy:

$$\frac{2V_{os}}{(1-\alpha)} = \frac{\sqrt{3}}{2}A \tag{8}$$

Further circuit analysis proves that setting α=0.2 allows to fit the slope of (7) near the three zero crossings. With α fixed, (8) shows that to maintain the correct zero crossings at different input power, V_{os} must be varied linearly with the input signal amplitude (A). Therefore, V_{os} is generated by an envelope detector, shown in the block diagram of Fig. 1.

In Fig. 4b the black solid line shows the DC trans-characteristic of the BJT implementation, well approximating the ideal curve in gray. Simulations at low frequency confirm that the circuit suppresses almost completely the component at f_0 in the output current. With a driving signal at 12.5GHz, device parasitic capacitors distort the dynamic shape of the trans-characteristic and reduce the f_0 suppression, but the issue can be solved by resonating out the equivalent shunt capacitance at the common-emitter node at frequency $2f_0$. To gain insight on the achievable f_0 rejection, simulated tripler output current is plotted versus V_{os} in Fig. 5. It can be observed

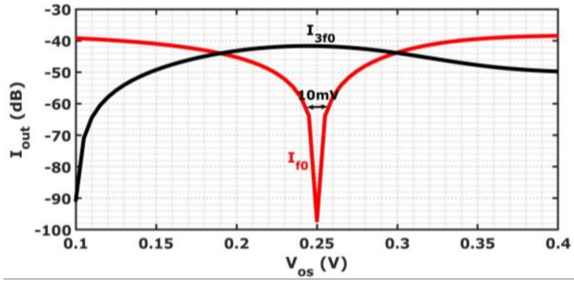


Fig. 5. Magnitude of the current components at f_0 and $3f_0$ versus V_{os}, derived from simulation with 12.5GHz input signal.

that the rejection is ultimately bounded by the accuracy to which V_{os} is set. At the optimal V_{os} the rejection is greater than 50dB, but remains above 20dB if V_{os} is set with +/-5mV accuracy.

Looking again at Fig. 4b, the dotted curve is obtained by plotting $I_{out}(t)$ against $V_{in}(t)$ from transient simulations at 12.5GHz input frequency of the implemented circuit, detailed in the next sub-section. The curve shows that the transistor implementation approximates well the ideal behavior also at high frequency.

B. Tripler Circuit Design

The complete tripler circuit is shows in Fig. 6. The differential signal provided by the transformer balun, T1, directly drives the base of $Q_{1,2}$ while it is attenuated by α through a capacitive voltage divider (C_1, C_2) to feed the base of $Q_{3,4}$. The four transistors have the same emitter area. The inductor L_{tail} resonates with the equivalent shunt capacitance at the common-emitter node and C_B is sized sufficiently large to act as an AC short. The quality factor of L_{tail} is not critical, because the impedance at resonance is limited by the equivalent resistance at the emitters of Q_{1-4}. The transformer T_2 provides the supply voltage and couples the tripler to the cascaded circuits. The transformer network is tuned to achieve a fractional bandwidth of 16%, centered at 37.5GHz.

V_{b2} and V_{b1} are the bias voltages for $Q_{1,2}$ and $Q_{3,4}$ respectively. They are generated by the envelope detector (ED) block such that V_{b1}-V_{b2} (corresponding to V_{os} in Fig. 4) tracks the amplitude of the driving signal. The ED circuit schematic is shown in Fig. 7. Q_{5-10} share the same base bias voltage, V_{CM}≈1.2, generated by a resistor string. In this way, $Q_{5,6}$ (driven by $V_{in}(t)$) and Q_7, set V_{RE} equal to the average value of $|V_{in}(t)|$. If $V_{in}(t)=A\sin(2\pi f_0 t)$, $V_{RE}=A/\pi$ and $I_{RE}=(A/\pi)/R_E$. $M_{1,2}$ mirror $I_{ref}+I_{RE}$ into R_2 while $M_{3,4}$ mirror I_{ref} into R_1 leading to $V_{b2}=V_{cc}-(I_{ref}+I_{RE})R_2$, $V_{b1}= V_{cc}-I_{ref}R_1$. Assuming $R_1=R_2$ results in $V_{os}=V_{b1}-V_{b2}=R_2 I_{RE} =(A/\pi)(R_2/R_E)$. The ratio R_2/R_E is selected such that V_{os} satisfies (8) with α=0.2, thus allowing to maintain good suppression of the fundamental frequency component independently from the amplitude of the input signal. All BJTs in Fig. 6 have an emitter area of 0.45x0.2μm^2, and R_2 and R_E are 4.5kΩ and 5.8kΩ, respectively. The total current consumption of the envelop detector is 600μA.

A first tripler chip has been realized [27] where a linear and wideband buffer, designed with the purpose of performing accurate experimental characterization, follows the tripler. The

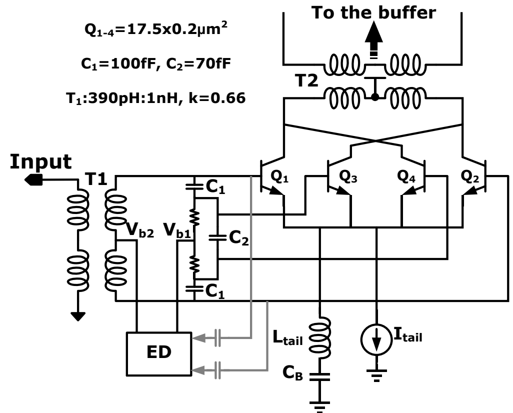


Fig. 6. Detailed schematics of the proposed tripler.

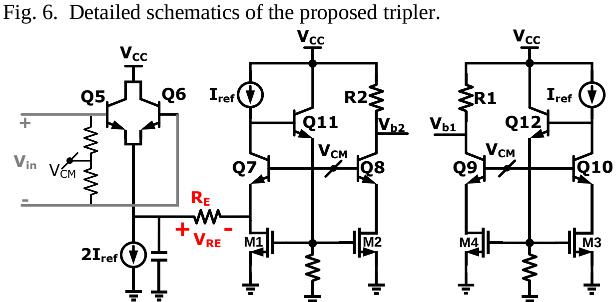


Fig. 7. Envelope detector circuit for adaptive biasing of the tripler core.

buffer is a resistively degenerated cascode differential pair with resistive load and peaking inductors. From simulations, it introduces 9.6dB voltage attenuation with flat bandwidth up 70GHz, allowing measurements up to the 5th harmonic of the input. The output power at 1dB gain compression point is 1dBm.

C. Tripler measurement results

The frequency tripler has been implemented in ST Microelectronics 55nm SiGe-BiCMOS technology. The on-chip buffer provides a differential output, but measurements are performed single-ended by probing each of the two outputs separately. Fig. 8 shows the measured power delivered to a 50Ω load at $3f_0$ and the leakage of f_0 and $5f_0$ versus frequency when the tripler is driven by a 0dBm input signal. The single-ended peak output power is 0dBm at 37.8GHz and remains within -3dB variation from 35 GHz to 41GHz, corresponding to 15.8% fractional bandwidth. In this frequency range, minimum and maximum rejection of f_0 are 39dB and 43.8dB. Minimum and maximum rejection of $5f_0$ are 37.5dB and 45.3dB , respectively. The tripler and ED draw 13.6mA from a 1.7V supply. The output buffer, not optimized for power efficiency but for wide bandwidth, high linearity and good common-mode rejection, draws 32mA from a 3V supply.

Fig. 9 shows the measured output power at $3f_0$ when the input power is swept at 12.5GHz. The same plot reports the total HRR considering up to $5f_0$. In the input power range –5dBm to 10dBm the single-ended output power at $3f_0$ rises from -8dBm to +4dBm. The HRR is better than 40dB until 4dBm input power and decreases to 36.6dB for 10dBm input power.

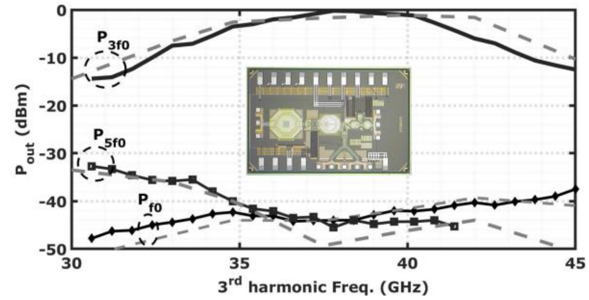


Fig. 8. Measured (solid) and simulated (dashed) tripler output power at the 3rd harmonic, fundamental, and the 5th harmonic versus frequency with 0dBm input signal. Chip photo is reported as inset [27].

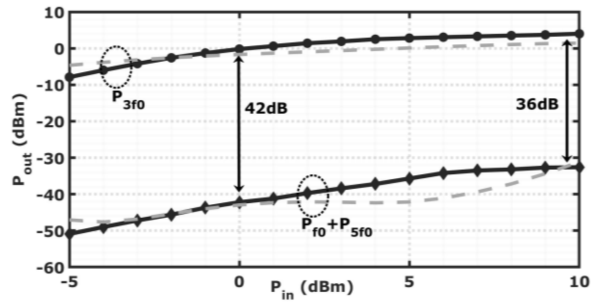


Fig. 9. Measured (solid) and simulated (dashed) output power of the tripler showing 3rd harmonic and HRR versus input power at f_0=12.5GHz.

In summary, measurement results confirms the excellent rejection of undesired harmonics by the proposed tripler and robust operation over wide interval of input signal power.

V. Frequency Doubler

Conventional frequency doublers are based on the push-push circuit configuration introduced in Sec. II, due to its simplicity and robustness. Considering the schematic drawn in Fig. 10a, where the bias current is set by I_{tail} and a large capacitor sets AC ground to the common-emitter node, provided the driving signals $V_{in}^{\pm}$ are perfectly differential, the input signal frequency and odd harmonics are intrinsically suppressed on the output current, I_{out}. However, if the inputs are not perfectly balanced, i.e. in the presence of amplitude mismatch and phase deviation from 180°, the common-mode component, at the fundamental frequency, is transferred to the output and amplified. This is the main issue limiting the rejection of the driving signal frequency component in the simple push-push doubler [28-30]. Moreover, the circuit topology in Fig. 10a generates a single-ended output, while a differential signal is often desirable in integrated transceivers. A balun transformer (e.g. coupled inductors [41, 42]) cascaded to the push-push pair can provide single-ended to differential conversion, but the interwinding parasitic capacitance impairs the amplitude and phase matching, particularly at mm-waves [43, 44].

The core of the proposed frequency doubler, shown in Fig. 10b, is based on a push-push transistor pair but produces a differential output current and it features enhanced robustness against amplitude and phase unbalance of the driving signals, thus improving substantially the rejection of the fundamental frequency component. The differential input signals $V_{in}^{\pm}$ drive the base of the push-push transistors $Q_{13,14}$ while the common-

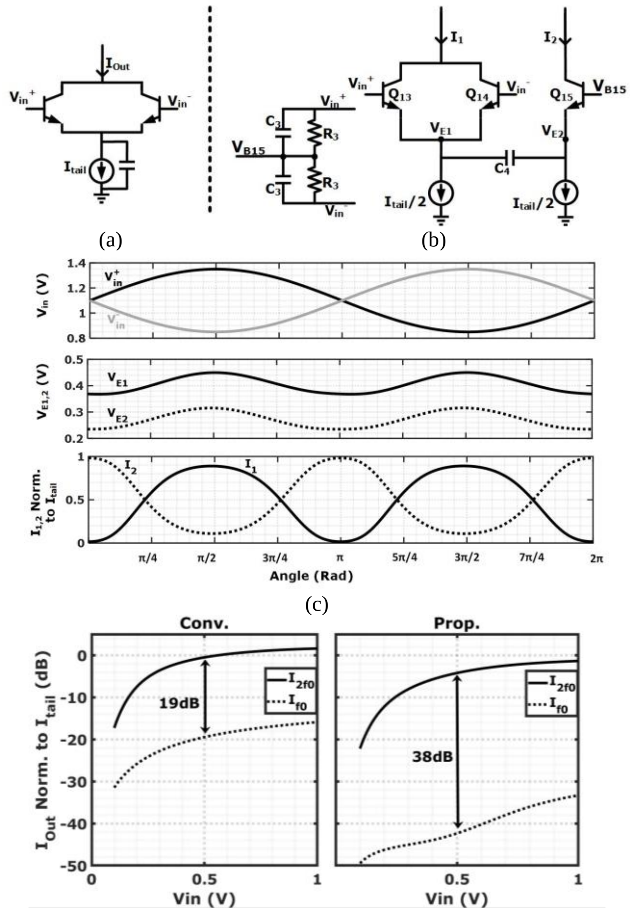


Fig. 10. (a) Schematics of a simple push-push doubler and (b) of the proposed doubler. (c) Time-domain waveforms. (d) Leakage of the fundamental component assuming 0.5dB amplitude and 5° phase imbalance on the driving signals.

mode voltage, extracted through the RC network in Fig. 10b, feeds the base of Q_{15}. As in the simple push-push doubler of Fig. 10a, the currents through Q_{13} and Q_{14} are composed of out-of-phase fundamental components (and odd-order harmonics) which cancel each other out, and in-phase 2nd harmonic components which add constructively to generate I_1 with a fundamental at twice the input frequency. The right branch of the circuit, with Q_{15} in common base, provides the differential output and enhances the robustness to amplitude and phase errors in $V_{in}^{\pm}$.

Assuming C_4 (400fF) is large enough to be a short circuit at the operation frequency, the emitter current of $Q_{13,14}$, I_1, flows into the emitter of Q_{15} and appears at its collector as I_2, with opposite phase of I_1, i.e. $I_2 = -I_1$. To gain further insight on circuit operation, the simulated voltage and current waveforms are reported in Fig. 10c. The top, middle and bottom plot show the input voltages $V_{in}^{\pm}$, the voltages at the emitters of $Q_{13,14}$ and Q_{15}, and the two output currents I_1,I_2. The tail bias current and the emitter area of Q_{15} are the same as $Q_{13,14}$. Therefore, at the quiescent point the emitter voltages V_{E1},V_{E2}, are equal. But when the input signal is applied, the emitter voltage of $Q_{13,14}$, V_{E1}, follows the envelope and its mean value (DC component) is shifted upward proportionally to the amplitude of V_{in}. This DC component is blocked by C_4 such that the mean value of V_{E2} remains the same as at the quiescent point, and thus $V_{E1} > V_{E2}$ (middle plot in Fig. 10c). In this way, whatever it is the input signal amplitude, $V_{BE\text{-}13,14} > V_{BE\text{-}15}$ near the peaks of $|V_{in}|$ ($\theta=\pi/2$ and $\theta=3/2\pi$ in Fig. 10c) while $V_{BE\text{-}15} > V_{BE\text{-}13,14}$ near the zero crossings of V_{in} ($\theta=0$, $\theta=\pi$ in Fig. 10c). Consequently, looking at the bottom plot in Fig. 10c, I_1~I_{tail} and I_2~0 near the peaks of V_{in} while I_2~I_{tail} and I_1=0 near the zero crossings of V_{in}.

With amplitude mismatch or phase deviation from 180° in $V_{in}^{\pm}$, a common-mode component at the input frequency drives the base terminals of the push-push transistors. For common mode, the simple push-push doubler in Fig. 10a behaves as a common-emitter stage, producing a large output signal leakage at the input frequency. In the proposed doubler the common-mode component on $V_{in}^{\pm}$, extracted by the RC network shown in Fig. 10b, feeds the base of Q_{15}. Therefore, for a common-mode input signal $Q_{13\text{-}14}$ and Q_{15} behave as a differential pair and do not transfer the common-mode input to the differential current I_1-I_2. To gain quantitative insight, Fig. 10d shows the simulated output current at twice the input frequency (I_{2f0}) and the leakage of the fundamental frequency (I_{f0}) with the simple push-push configuration of Fig. 10a and with the proposed doubler versus the input amplitude. The two circuits are designed with the same area of the input transistors and total bias current. 0.5dB amplitude imbalance and 5° phase error from 180° between V_{in}^{+} and V_{in}^{-} are assumed, leading to a leakage of I_{f0} 19dB below I_{2f0} in the simple push-push configuration. With the proposed frequency doubler the suppression of I_{f0} is raised to 38dB. From Fig. 10d the magnitude of I_{2f0} in the proposed solution is reduced by 3.5dB. However, the penalty is less than the insertion loss of a typical passive filter that can exert the same

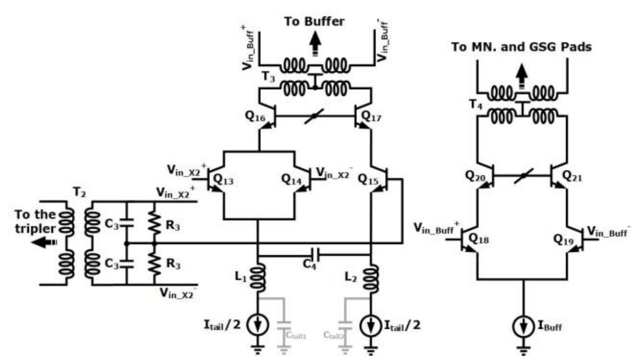


Fig. 11. Complete schematics of the doubler and the output buffer.

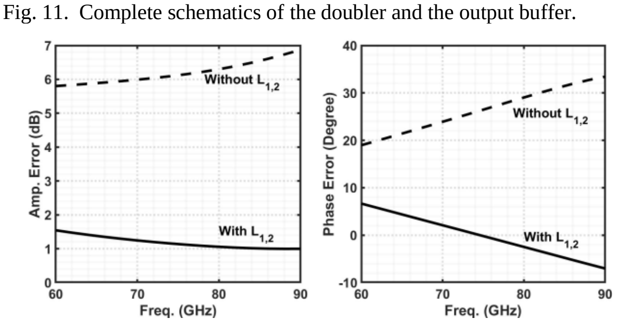


Fig. 12. Simulated amplitude and phase errors of the differential doubler output with and without $L_{1,2}$.

amount of harmonic rejection, not considering the area occupation. Moreover, the proposed solution offers a differential output which is often desirable in integrated transceivers.

Fig. 11 shows the complete schematic of the frequency doubler and the output buffer. The input signal, generated by the tripler, is coupled with a transformer T_2 (260pH primary, 360pH secondary, with k=0.26) where at the secondary, C_3=75fF senses the input common-mode and generates the base voltage of Q_{15}. The DC bias voltage (1.1V) is applied through R_3. Common-base transistors are stacked on $Q_{13,14}$ and Q_{15} to mitigate the impact of miller capacitances. $Q_{13,14}$, working in class C, have an emitter area of 5x0.2μm^2, and $Q_{15\text{-}17}$ have double that size. The differential output current feeds the primary winding of a transformer T_3, used to couple the doubler to the output buffer and has an equivalent inductance of 100pH at its both primary and secondary with a coupling factor of 0.39.

The parasitic capacitances of the tail current sources, $C_{tail1,2}$, are around 70fF each, which is not negligible at the operating frequency. They appear in parallel to the signal path of the second harmonic current flowing from the emitter of $Q_{13,14}$ to the emitter of Q_{15}, causing reduction of the conversion gain and amplitude and phase unbalance between the two output currents. Therefore, as shown in Fig. 11, two sufficiently large inductors (225pH), $L_{1,2}$, are placed in series with the current sources rising the impedance at the operating frequency and thus shielding the effect of $C_{tail1,2}$. Fig. 12 shows the simulated amplitude mismatch and phase deviation from 180° in the doubler output currents with and without $L_{1,2}$. Across the 60GHz to 90GHz output frequency range, the inductors reduce the amplitude mismatch from 6-7dB down to less than 1.5dB and the phase error from 20-35° down to ±7°.

From simulations, the amplitude mismatch and phase deviation from 180° of the currents delivered by the doubler active core are within 1.5dB and +/-7°, respectively, across the 60GHz to 90GHz output frequency range.

The secondary of the transformer T_3 drives the output buffer. The input transistors $Q_{18,19}$ and the common-base transistors $Q_{20,21}$ form a cascode differential amplifier. They all have the same emitter area of 10x0.2μm^2. The transformer T_4 and a passive network toward the output pad provide matching to a 50Ω load and differential to single-ended conversion for measurements with a GSG probe.

VI. Sextupler Simulations

The frequency sextupler comprises the cascade of the tripler and doubler with output buffer, as shown by the block diagram in Fig.1. Compared to the first version of the tripler, in the test-chip described in Sec. IV [27], the tripler in the sextupler has been optimized to limit power consumption. In particular, the core supply voltage is reduced from 1.7V to 1.2V, as some voltage headroom was wasted in the first design, and the bias current is scaled down, from 13mA to 8mA, because the tripler's load to be driven in the sextupler chain is smaller than in the test-chip for the tripler alone. The doubler and output buffer following the tripler have been described in Sec. V.

From simulations with an input signal at f_0=12.5GHz, the saturated output power of the sextupler ate $6f_0$=75GHz, limited by the final buffer, is P_{out}=5.5dBm, with input power of -3dBm. This corresponds to a maximum conversion gain of 8.5dB. Simulations of the harmonic rejections along the chain are also performed and summarized in Table I. The first, second and third column report the HRR for different harmonics at the tripler, doubler and buffer output, with the desired output signal at $6f_0$=75GHz. Simulations are also compared with the polynomial modelling considered for the analysis in Sec. III. From the simulation results in the first column of Table I, the tripler output can be approximated as:

Table I. Simulation of HRR along the sextupler chain (within parentheses, in the second column, are reported calculated values)

Tripler output	Doubler output (calculations in parentheses)	Buffer output
$\frac{H_3}{H_1} = 46.5dB$	$\frac{H_6}{H_3} = 40.7dB$ (40.7)	$\frac{H_6}{H_3} = 53.1dB$
$\frac{H_3}{H_2} = 58.9dB$	$\frac{H_6}{H_4} = 44.1dB$ (40.4)	$\frac{H_6}{H_4} = 49.5dB$
$\frac{H_3}{H_4} = 59.3dB$	$\frac{H_6}{H_5} = 52.5dB$ (52.7)	$\frac{H_6}{H_5} = 60.8dB$
$\frac{H_3}{H_5} = 40\ dB$	$\frac{H_6}{H_7} = 55.1dB$ (53)	$\frac{H_6}{H_7} = 67dB$
	$\frac{H_6}{H_8} = 34.5dB$ (33.9)	$\frac{H_6}{H_8} = 51.7dB$

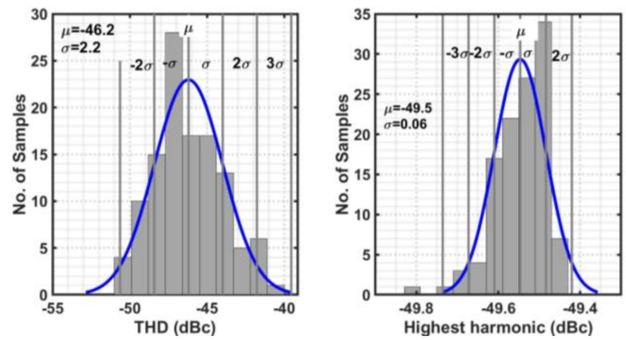


Fig. 13. Result of Monte Carlo simulations showing the spread of THD and the highest undesired harmonic.

$$w \approx \frac{H_1}{H_3}\cos(\omega_0 t) + \frac{H_2}{H_3}\cos(2\omega_0 t) + \cos(3\omega_0 t) + \frac{H_4}{H_3}\cos(4\omega_0 t) + \frac{H_5}{H_3}\cos(5\omega_0 t) \quad (9)$$

with $\omega_0 = 2\pi f_0$.

The values within parentheses in the second column of Table I are calculated modeling the doubler with (1) if the input signal is given by (9). The parameter ρ in (1), determining the finite rejection of the fundamental component at the doubler output (which, for the doubler after the tripler, corresponds to $3f_0$) , is estimated from the simulated H_6/H_3 of 40.7dB, leading to ρ=108. Calculations agree well with the simulated HRR, with only few dBs of error. Despite the approximations in the modeling approach introduced in Sec. III (neglecting e.g. higher order terms in the polynomial and memory effects), it still provides a good first order approximation of the unwanted harmonic levels.

Interestingly, considering even and odd harmonics at the tripler output and only a second-order polynomial model for the doubler, all the undesired output harmonics, up to the 8th are well predicted. As mentioned in footnote 1 in page 4, the 7th harmonic appears at the doubler output if the tripler output is not perfectly balanced and the doubler is fed by even harmonics (the 4th in particular).

Finally, to investigate the resiliency of the sextupler to process variation and mismatches, Monte Carlo simulations have been performed on the full chip. Fig.13 shows the results with a 0dBm input at 12.5GHz. The suppression of the largest unwanted harmonic and the total harmonic rejection at 3σ are -49.5dBc and -39.6dBc respectively.

VII. Measurement Results

A photograph of the sextupler chip, fabricated in ST Microelectronics 55nm SiGe-BiCMOS technology, is shown in Fig. 14 and measures 810μm by 1440μm including all the signal and supply pads. The supply voltage for the tripler core is 1.2V, and for the ED, doubler and the buffer stage it is 1.7V. The current consumption of the tripler, ED, doubler and output buffer are 8mA, 0.6mA, 7.9mA, and 23mA, respectively. Fig. 15 shows the simulated and measured power delivered to a 50Ω load at 6f_0 and leakage of other harmonics of f_0 versus frequency when the sextupler is driven by a 0dBm input signal. The peak output power, P_{out}, is 5.6dBm at 72GHz corresponding to a power conversion efficiency, $\eta = P_{out}/(P_{DC}+P_{in}) = 5.6\%$. The frequency component at 6f_0 remains above 0dBm from 64.7GHz to 84.7GHz, corresponding to a 26.8% BW, where the suppression of unwanted harmonics is better than 35dB. Moreover, P_{out} remains within 3dB variation from 65.9GHz to 78.6GHz, corresponding to 17.6% fractional BW. In this frequency range, the unwanted harmonics of the input are suppressed by more than 38.5dB. Consistent results are achieved by measurements repeated on different samples.

Overall, simulations and measurements in Fig. 15 are in good agreement. The largest discrepancy is on the 5th and 7th harmonics. As explained in Sec. VI, they arise from even harmonics at the output of tripler (nominally balanced) due to imbalances and asymmetries in the differential circuits and components (input balun, transformers) which are particularly difficult to be precisely modeled. The rapid increase of these harmonics at the edges of the band is expected also from simulations and it is attributed to the frequency response of the interstage band-pass networks ($T_{2\text{-}4}$ in Fig. 11). As an example, the simulated suppression of the 7th harmonic in Fig. 15 drops from 67dB when the input signal is at center frequency, f_0=12.5GHz (6f_0=75GHz) to 15dB when f_0=10GHz (6f_0=60GHz). 7f_0 results from the beating of 3f_0 and the leakage of 4f_0 at the tripler output. With f_0 reduced to 10GHz, the desired signal at 3f_0 moves below the passband of T_2 while 4f_0 moves closer to its center frequency. As a result, H_3/H_4 ratio is reduced (by ~20dB). Following the analysis of Sec. III, it can be shown that this in turn results in the same reduction of H_6/H_7 at the doubler output. After the doubler, 6f_0 moves below the passband of T_3 and T_4 while 7f_0 is more close to the center frequency, hence the H_6/H_7 ratio degrades (~15dB through T_3 and ~15dB though the buffer and T_4). Therefore, it is expected

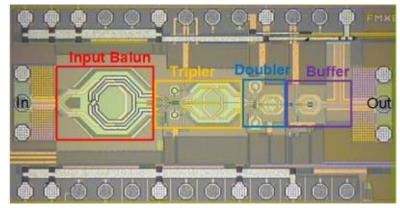


Fig. 14. Chip photograph of the frequency sextupler.

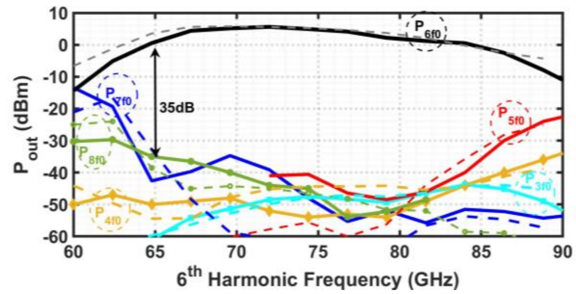


Fig. 15. Measured (solid) and simulated (dashed) output power of the 6th harmonic and of undesired harmonics versus frequency for 0dBm input signal.

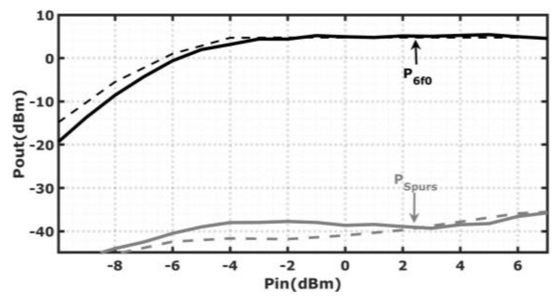


Fig. 16. Measured (solid) and simulated (dashed) output power of the 6rd harmonic (P_{6fo}) and all the unwanted harmonics (P_{Spurs}) at f_0=12.4GHz.

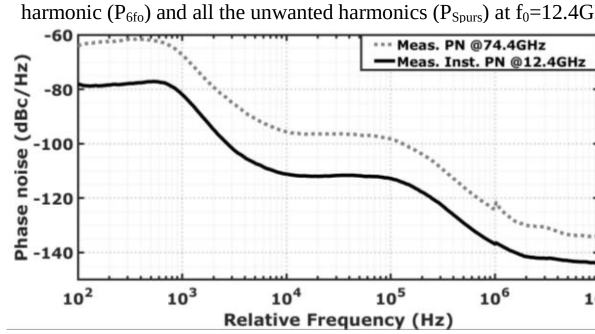


Fig. 17. Measured input and output phase noise.

that H_6/H_7 reduces by around 50dB. Nevertheless, in the bandwidth of interest, all unwanted harmonics, including the 5th and 7th, are heavily suppressed.

Fig. 16 shows the simulated and measured output power at 6f_0 when the input power is swept at 12.4GHz. The same plot reports the total power of unwanted harmonics. The output saturates when the input power reaches -3dBm, and from -3dBm to 7 dBm, the variation of the output power is within 1dB. The total HRR is better than 40dB for input power larger than -5.5dBm.

Fig. 17 shows the phase noise at the input and output of the sextupler when the output frequency is 74.4GHz. The difference between the two plots is 15.5dB, as expected by the frequency multiplication by 6, proving negligible phase noise

Table II. Measurement summary and comparison of the sextupler chip with other frequency multipliers in the same frequency range.

Ref	***Tech***	***×N***	***f_{out} (GHz)***	***Supp. of Harm. (dB)***	***P_{out} (dBm)***	***Conv. Gain (dB)***	***P_{DC} (mW)***	***η (%)***
[17]	65nm CMOS	9	88-99.5 (12.2%)	31	8.5	-5.7	438	1.5
[45]	65nm CMOS	9	88.9-95.5 (7.2%)	16	-1.8	1.4	120	0.55
[46]	100nm pHEMT	8	90.5-95.2 (5%)	21	-0.4	-0.6	138	0.65
[47]	65nm CMOS	8	84-98.4 (15.3%)	10	-7.12	-7.12	1	9.7
[48]	90nm CMOS	6	96.1-98.4 (2.3%)	NA	-17.2	-17.2	55.4	0.04
[49]	100nm HEMT	6	155-195 (22.8%)	20	0	-6.5	92.5	1
[50]	65nm CMOS	6	74.7-82.2 (9.6%)	NA	4	4	51	4.8
[16]	100nm HEMT	6	78-104 (28.6%)	25	7	5	470	1
[51]	SiGe BiCMOS	4	70-110 (44.5%)	30	3	3	170	1.17
[52]	SiGe BiCMOS	4	62-76 (20%)	33	9	NA	262	~3
[53]	SiGe BiCMOS	4	99-132 (28.6%)	25	8.5	8.5	79	8.8
[54]	SiGe BiCMOS	3	69-86 (22%)	33	9.9	7.9	158	6.12
[32]	SiGe BiCMOS	3	80-100 (20%)	20	-10.5	-10.5	75	0.12
[36]	SiGe BiCMOS	3	48-58 (19%)	28	9.5	12	220	4
[55]	0.15um HEMT	3	58.5-65 (10.5%)	19	-0.4	-4.4	52	1.67
[56]	65nm CMOS	3	57-78 (31%)	20	-3.7	1.3	60	0.7
This work	SiGe BiCMOS	6	65.9-78.6 (17.6%)*	>38.5	5.6	5.6***	63.1	5.66
This work	SiGe BiCMOS	6	64.7-84.7 (26.8%)**	>35	5.6	5.6***	63.1	5.66

*-3dB BW
**>0dBm
*** at center frequency, with 0dBm input power. The maximum conversion gain is 8.5dB with Pin=-3dBm

deterioration from the sextupler chain.

Finally, measurement results are summarized in Table II and compared against previously reported frequency multipliers with similar output frequency. The presented frequency sextupler achieves bandwidth and output power aligned with state of the art, but with excellent power efficiency and the highest suppression of undesired harmonics of at least 35dB. Among other works, the highest reported suppression is around 30dB, achieved by the quadruplers in [51, 52] and the multiplier by 9 in [17] with 3x or more higher power consumption and lower power efficiency, and by a tripler alone in [54]. Also the quadrupler in [53] has a remarkable efficiency while maintaining high output power and bandwidth, but a simulated harmonic suppression of only 25dB.

VIII. Conclusion

A frequency sextupler with novel tripler and doubler circuit topologies featuring enhanced suppression of unwanted harmonics has been presented. The tripler core is devised to reproduce the trans-characteristic of a 3rd order polynomial that ideally generates only the 3rd harmonic of a sinusoidal input signal. The operation is robust against variation of the input signal power thanks to an adaptive biasing circuit implemented with an envelope detector. The frequency doubler is an evolution of the push-push topology modified to produce a differential output current and to improve the robustness against amplitude and phase unbalances of the driving signals, thus improving substantially the rejection of the fundamental frequency component. Implemented in a 55nm SiGe-BiCMOS technology with 63.1mW total power dissipation, the sextupler circuit achieves bandwidth and output power aligned with state of the art, but with excellent rejection of undesired harmonic components and power efficiency.

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