A D-Band 16-Element Phased-Array Transceiver in 55-nm BiCMOS

David del Rio, Juan F. Sevillano, Rolando Torres, Andoni Irizar, Pascal Roux, Mahmoud Pirbazari, Andrea Mazzanti, Jussi Säily, Antti Lamminen, Jesús de Cos, Mario G. Frecassetti, Maurizio Moretto, Andrea Pallotta and Vladimir Ermolov

***Abstract*—A 16-element 140-160-GHz phased array transceiver is reported. The chipset is fabricated using STMicroelectronics' 55-nm SiGe BiCMOS process. 5 different chips are implemented: a 4-channel transmitter with a maximum gain per channel of 15 dB and 0-dBm saturated output power; a 4-channel receiver with a maximum gain of 8 dB, a -10.4-dBm input 1-dB compression point (IP_{1dB}) and a minimum noise figure of 15.6 dB per channel; a 0-1-GHz to 140-160-GHz I/Q up-converter with integrated frequency doubler, exhibiting a -13.5-dB conversion gain (CG) and -6-dBm output 1-dB compression point using a 70-80-GHz local oscillator (LO); a 140-160-GHz to 0-1-GHz I/Q down-converter with integrated frequency doubler, exhibiting a CG of 0 dB and IP_{1dB} of 0 dBm using a 70-80-GHz LO and an 11.67-13.33-GHz to 70-80-GHz x6 frequency multiplier for the LO, delivering 5.6-dBm maximum output power. The chips are assembled together with 16 cavity-backed aperture-coupled patch antennas using a high-performance and low-cost commercial PCB, supported over a heat sink. The main challenges encountered during the integration of the proposed system are also discussed. The complete system is used to build a wireless radio link in the laboratory, demonstrating 2-dimensional beam steering in a range of $\pm 30^{\circ}$.**

***Index Terms*—BiCMOS, phased array, millimeter-wave, RFIC, D-Band, beam steering.**

I. Introduction

The high mm-wave and sub-THz regions of the electromagnetic spectrum offer the vast available bandwidth required to meet the exponentially growing capacity demands in wireless backhaul networks. The D-band, which ranges from 130 to 170 GHz, is particularly being considered as a suitable candidate for the implementation of high-capacity radio links for 5G and beyond [1]–[3].

To reduce the deployment and operation costs of such high-capacity front and backhaul radio links, reconfigurable mesh networks with bi-dimensional beam alignment/steering functionalities and supporting flexible frequency division duplexing (fFDD) are desired [4]. By independently changing the phase of the signal fed into each antenna, phased array transceivers offer this beam steering functionality, together with an enhancement of the directivity, radiated power and receiver sensitivity due to the spatial combination. Additionally, owing to the high operation frequencies in the high mm-wave part of the spectrum, a large number of elements can be placed in a compact area. Developments in modern CMOS and BiCMOS technologies, with f_T in excess of 200 GHz and the capability to integrate RF blocks together with advanced built-in self-test (BIST), digital control and calibration subsystems, are paving the way for the design of integrated D-band phased array transceivers [5], [6].

However, there are still some issues to be resolved when building integrated mm-wave phased array systems. On the one hand, working near the f_T of the technology involves dealing with low gain and efficiency in circuits. This requires a large circuit area and DC power to achieve high gain and output power, which consequently stresses the DC bias and thermal management systems. On the other hand, it is necessary to carefully choose and design the most appropriate assembly technology and integration platform to provide low losses at a low cost [7].

Moreover, the small wavelength associated to the high mm-wave part of the spectrum entails an extra challenge related to the phased-array circuit size. To provide scanning capabilities in both the azimuth and elevation planes (2D) together with a frequency-independent behavior, each antenna element in the array must be driven independently. As the optimum $\lambda/2$ pitch between antenna elements is 1 mm at 150 GHz, the dimensions of each transmitter or receiver channel need to be compatible with that size to ensure the desired 2D scanning features. This makes the circuit area critical, requiring a careful trade-off with other parameters such as output power and gain.

To the date, several mm-wave integrated phased array transceivers have been successfully demonstrated in frequencies below 100 GHz. [8] and [9] report 16-element and 256-element receiver and transmitters at 60 GHz, respectively, while [10] describes a complete 94-GHz system with up to 384 elements. Above 120 GHz, the reported works are more scarce. [11] proposes a 140-GHz phased array with 4 transmitting and 4 receiving antennas, driven in groups of 2 antennas by single-chain TX and RX dies. A 139-157-GHz

D. del Rio, J. F. Sevillano, R. Torres and A. Irizar are with Ceit-Basque Research and Technology Alliance (BRTA), 20018 Donostia - San Sebastian, Spain, and with Tecnun, University of Navarra, 20018 Donostia - San Sebastian, Spain. Email: ddelrio@ceit.es

P. Roux is with Nokia-Bell-Labs France, 91620 Nozay, France.

M. Pirbazari and A. Mazzanti are with the Department of Industrial and Information Engineering, University of Pavia, 27100 Pavia, Italy.

A. Lamminen, J. Säily and V. Ermolov are with VTT Technical Research Centre of Finland, 02044 Espoo, Finland.

J. de Cos is with ERZIA Aerospace and Defense, ERZIA Technologies, 39012 Santander, Spain.

M. G. Frecassetti and M. Moretto are with Nokia X-Haul BU, 20871 Vimercate, Italy.

A. Pallotta is with STMicroelectronics, 20010 Cornaredo, Italy.

This research work has received funding from the European Union's Horizon 2020 Research and Innovation Program under grant no. 761390, project acronym: DREAM, and under grant no. 955699, project acronym: DRAGON.

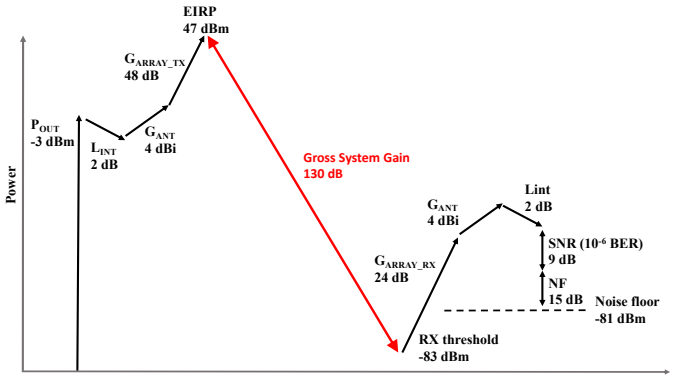


Fig. 1. System level diagram.

transmitter connected to a 2x2 fixed antenna array using a commercial PCB technology has been reported in [12]. Recently, a 8 × 16-element 150-GHz phased array system has been reported in [13], which uses 8 single-channel ICs, each with a phase shifter + PA or LNA + phase shifter chain, to drive 8 sub-arrays, each with 16 antenna elements. Reported simulation results demonstrate ±15° beam steering in one plane. The system is packaged using a novel radio-on-glass technology. The same technology is used in [14] to show simulations of 2D beam steering with 256 antenna elements.

In this work, an integrated 16-element 140-160-GHz phased array transceiver is reported, which employs compact 4-channel TX/RX BiCMOS ICs. The presented approach allows driving each antenna element independently, thus providing wideband and bidirectional beam steering capabilities, as well as the possibility to scale the system to drive larger arrays. The TX and RX dies are connected to the 16 antenna elements and assembled together with I/Q up and down-converters and LO frequency multipliers, using a high-performance and low-cost commercial PCB technology. To the best of our knowledge, it is the first time that a complete phased array transceiver system, integrated on a low-cost commercial PCB platform and experimentally demonstrating 2D beam steering at D-band frequencies has been reported. The implemented prototype also allows investigating and evaluating critical challenges associated to the system integration.

The rest of the paper is organized as follows: Section II presents the link budget analysis and system specification, outlining the proposed system architecture. Section III presents the detailed design of the chips, while section IV shows their on-wafer measured performance. Section V describes the integration platform, including the antennas for the array, while section VI presents over-the-air tests. Finally, section VII summarizes the main conclusions of the article.

II. System Architecture

Previous studies have shown that the >50 Gbps data rates required by future backaul networks can only be achieved by the use of MIMO schemes (typically 2x2), together with a flexible and efficient use of the available spectrum [15]. As the regulation for the D-Band provides portions of unequal bandwidths within the band [3], for instance 7.25 GHz at

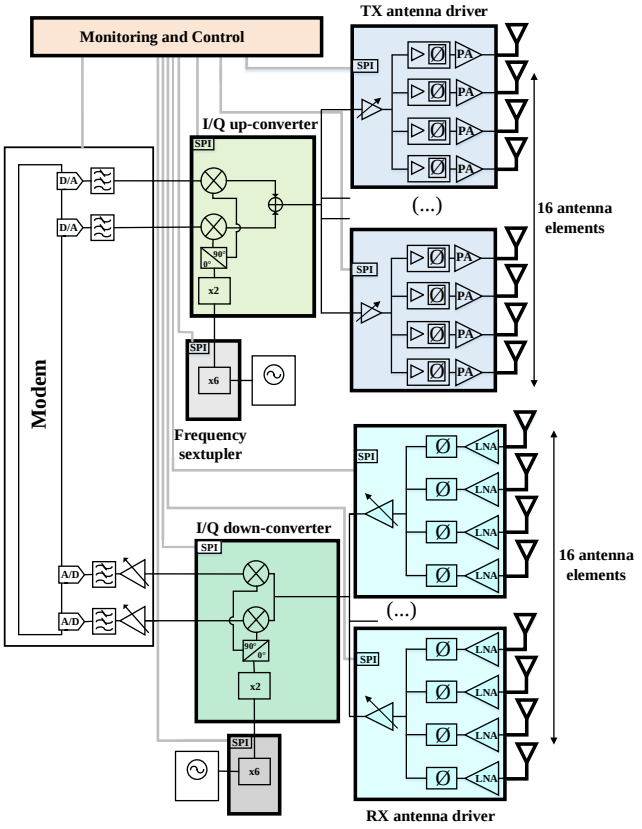


Fig. 2. Proposed transceiver architecture.

140 GHz and 12.25 GHz at 150 GHz, it is not efficient to adopt traditional frequency arrangements where a portion of the spectrum is always used in the TX and another portion in the RX, isolated using a diplexer. By contrast, diplexer-less flexible frequency division duplex schemes (fFDD), where TX and RX channels can be located anywhere in the available band, are preferred at D-band frequencies. As for the channels, a maximum channel bandwidth of 2 GHz is considered a good compromise, given the limitations of IF/baseband components and commercial modems. This bandwidth also ensures a fair usage of the shared spectrum among different operators. In each channel, it is theoretically possible to transmit raw data rates between 2 Gbps and 16 Gbps, using modulation schemes from BPSK to 256-QAM. Therefore, it is necessary that the transceiver chipsets for such links provide a very wide RF operation bandwidth, ideally covering the whole D-band, while maintaining baseband bandwidths of at least 1 GHz.

Regarding the path length, it is expected that future high-capacity backhaul links will be located in urban environments, with a link distance of no more than 300 m in 90% of the cases [15]. For this distance, a path loss in the order of 130 dB should be addressed to ensure > 99.9% availability under heavy rain conditions [16]. Consequently, wireless systems for D-band point-to-point backhaul links should provide a gross system gain of at least 130 dB at the wanted operation conditions (modulation & channel size). The gross system gain is defined as the difference between the radiated power at the TX side (EIRP) and the minimum

received signal level at the RX for having a bit error rate (BER) better than typically 10^{-6} (threshold). The specifications for the different transceiver elements can be derived using a level diagram as the one shown in Fig. 1. The analysis assumes a typically required SNR of 9 dB at 10^{-6} BER, for the case of QPSK modulation in a 2-GHz channel. The requirements are fulfilled with a linear output power of -3 dBm at the PA output, a noise figure (NF) of 15 dB at the receiver LNA input and 2-dB losses between chip and antennas. To increase the system gain and at the same time provide reconfigurability of the radiation direction and help in the initial set up, a phased array system is proposed, where each antenna element is connected to a PA/LNA to ensure frequency-independent 2D beam steering capabilities. At the transmitter side, the EIRP grows with the square of the number of antenna elements, as both the directivity and effective output power depend on the number of antennas –the quantity of PAs grows with the number of antennas. On the receiver side, the sensitivity improves linearly with the number of antennas, due to the SNR enhancement provided by coherent combination of received signals and incoherent combination of noise. It can be shown that the required gross system gain can be achieved when at least 256 antennas are employed, assumming a typical 4-dBi gain per antenna element. For higher modulation orders, requiring higher SNR, the link could maintain the gross system gain if more antennas were used.

In this work, a complete chipset for a phased array and an integration platform using a commercial PCB technology are proposed for this envisaged D-band transceiver. As a first step, a down-scaled subset with fewer antenna elements (16) but with all the desired functionalities, like beam steering in azimuth and elevation planes, is implemented and experimentally demonstrated. This implementation makes it possible to demonstrate the functionalities and to investigate the integration platform assembly challenges.

The phased-array architecture shown in Fig. 2 is proposed for the transceiver, where the blocks implemented in this work are highlighted with thick borders. To enable the adoption of a flexible frequency division duplex (fFDD) scheme and avoid the need for lossy diplexers or TX/RX switches, separate antenna arrays are used for the transmitter and receiver.

A direct-conversion scheme is employed, where the local oscillator (LO) signal is converted to D-band by means of two frequency multiplication steps. An X-band LO is first multiplied by 6 inside a dedicated chip implementing a frequency sextupler, while a frequency doubler is implemented inside the I/Q up- and down-converter chips. Beamforming is performed with phase shifters in the RF chain [7], [17], so that the phase of the RF signal reaching each antenna can be changed independently.

As mentioned in Section I, since each antenna element in the array needs to be addressed independently to provide 2D scanning capabilities, circuit size plays a crucial role and impacts many design choices –the λ/2 pitch between antennas is 1 mm at 150 GHz. Four transmitter/receiver chains are implemented in each antenna driver chip, which allows saving several DC and digital control pads, thus leaving more chip area for the active circuits, as well as a less dense routing in the integration PCB with respect to a single-channel-chip approach. Moreover, with a 4-channel chip configuration the DC current consumption and thermal dissipation in each chip are still maintained at manageable levels. In addition, the total number of variable-gain amplifiers, required to accommodate for different working conditions and array sizes, is divided by four. The proposed multi-chip approach opens the possibility to scale the system to drive arrays with different number of antennas, depending on the number of employed dies.

A 50-Ω reference impedance is chosen as interface between building blocks and between chips, which facilitates the integration as well as standalone tests with little modifications. The dies are mounted on a low-loss substrate, were the antennas are also constructed. As it can be seen in Fig. 2, all the ICs in the system implement SPI slaves. This SPI slave provides a digital interface for beam steering control and settings configuration of the chips [18]. More details about the integration platform are given in Section V.

The baseband

III. Chipset design

This section will discuss the design of the different chips for the phased array transceiver. They are all implemented using a commercial 55-nm BiCMOS process provided by STMicroelectronics, which features high-speed bipolar transistors with f_T of 320 GHz [19].

The colored subsystems in Fig. 2 correspond to the different implemented ICs: the 4-channel transmitter and receiver, the I/Q up- and down-converters and the frequency multiplier. As mentioned, they are controlled using integrated SPI slaves, each addressing 12×8-bit write registers and 4×8-bit read registers [18] and occupying only 85 μm x 85 μm.

A. 4-channel transmitter

As shown in Fig. 2, the transmitter chip consists of a VGA, a four-way splitter and four identical chains made of a driver, a phase shifter and a PA.

The VGA is implemented using two cascaded stages, each based on the variable-gain distributed amplifier (VGDA) reported in [20]. A distributed structure with a flat and wide bandwidth is chosen for this stage, which leaves more room in terms of RF bandwidth for critical blocks such as the PA. Standalone measurements of a single VGA stage show a gain of 6 dB at 150 GHz and values higher than 3 dB up to 160 GHz, with a gain control range wider than 20 dB. The gain ripple is better than $\pm$0.2 dB over a 2-GHz bandwidth, while the IP1dB is better than -10 dBm over the full control range of 20 dB, guaranteeing that the signal quality is not affected by the gain reduction.

As for the 4-way splitter, it is desired that it provides low insertion loss, wide bandwidth, good impedance matching and high isolation between outputs, while occupying a small area. Therefore, a 4-way Wilkinson splitter has been implemented, where the λ/4 lines have been compacted by giving them a spiral shape. A 3D view of the structure is shown in Fig. 3. As observed, its compact area of 100 μm x 150 μm, together with the fact that the input and output ports are symmetrically

placed at the periphery, make it easy to integrate the splitter at the center of the TX array chip. EM simulations of this structure show an insertion loss of 2 dB, apart from the 6 dB due to 4-way power splitting, with a value lower than 5 dB up to 200 GHz. The imbalance between ports is better than 0.15 dB due to the symmetrical layout, while the simulated isolation is better than 20 dB from 130 to 180 GHz.

A wideband and compact driver amplifier is placed to compensate the losses of the power splitting without degrading the linearity, keeping the signal level more or less constant along the chain. The schematic of the driver is shown in Fig. 4. It consists of a cascode stage (Q1,Q2), followed by a common-emitter (CE) stage (Q3), to simultaneously get a good return loss at the maximum output power and a compact layout. The inter-stage matching network is made of three lines (L2, L3, L4) and two feedback resistors (R1, R2), which help optimizing the bandwidth, flatness and gain. A 75-Ω series transmission line (L5) is placed at the input to provide a wideband impedance matching while maintaining a compact layout. A small series resistor is placed in the Vcc path to enhance the stability and robustness against environmental variations, which might happen when integrating the amplifier with other circuits in the 4-channel antenna driver chips. A value of 16-Ω value provides a good compromise between robustness and RF performance. Standalone measurements of the driver show a gain of around 8 dB in the D-band. The measured OP1dB is better than -1 dBm and the saturated output power is better than 1 dBm from 140 to 170 GHz.

The phase shifter is designed using an active vector-modulator architecture [21]–[24], based on the circuit reported in [24]. To support the integration in the complete phased array system addressed in this work, the analog control current sources have been substituted by 8-bit current-steering DACs [18].

Regarding the power amplifier design, as one PA is intended to drive each antenna element, placed 1-mm apart ($\lambda/2$ at 150 GHz), the compactness is a main driving factor in its design, at the cost of other aspects like the maximum output power, which would require combining several stages in a bigger area. The schematic of the circuit is shown in Fig. 5, which is preceded by two driver stages like the ones presented above. It is based on a single-ended common-emitter configuration, for improved output matching, drain efficiency and compactness. The use of a single-ended architecture, however, implies a higher sensitivity to load mismatches and non-idealities of the Vcc/ground connections. Therefore, these aspects need to be carefully managed at the integration and assembly stages. The PA is made of three cascaded stages, such that the maximum output power is not limited by the preceding driver. The core size (3 stages) is 0.6 mm x 0.16 mm. Standalone measurements at room temperature of a single PA stage show a nominal small-signal gain bigger than 5 dB from 130 to 160 GHz, with an OP1dB of 5 dBm and an input return loss better than 10 dB.

B. 4-channel receiver

The 4-channel receiver chip, as observed in Fig. 2, consists of four identical chains made of an LNA and a phase shifter,

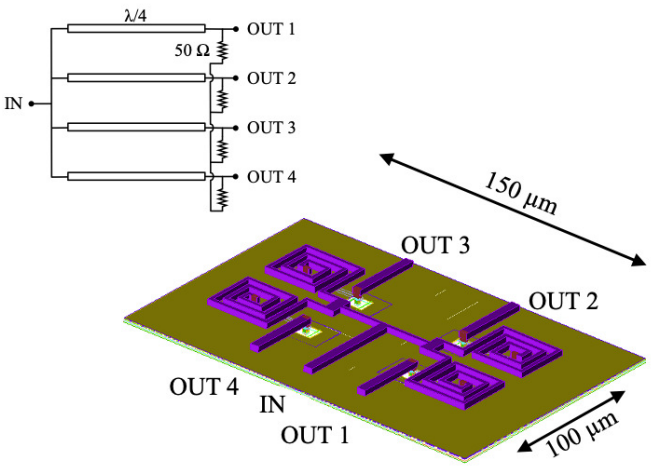


Fig. 3. 3D view of the implemented 4-way splitter.

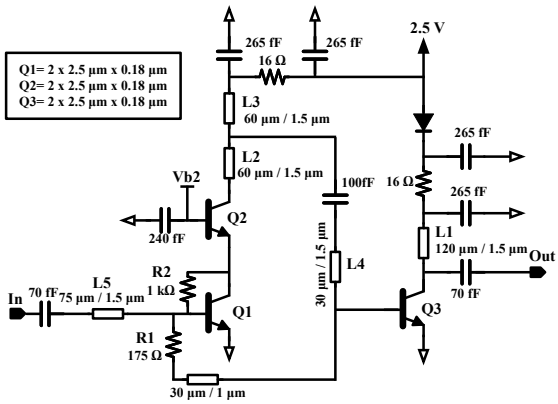


Fig. 4. Schematic of the proposed driver.

followed by a power combiner and a VGA. The phase shifter, power combiner and VGA designs are the same as the ones presented for the transmitter in Section III-A, just modifying their matching networks.

With regard to the LNA, it has been designed to be compact and unconditionally stable, as it is directly connected to each antenna element. Its schematic is shown in Fig. 6. The architecture is based on the driver amplifier described before, with some adjustments to improve the noise figure without degrading the input return loss. The transmission lines L5 and L6 are used to provide simultaneous noise and input power matching. Standalone measurements of the LNA show a gain

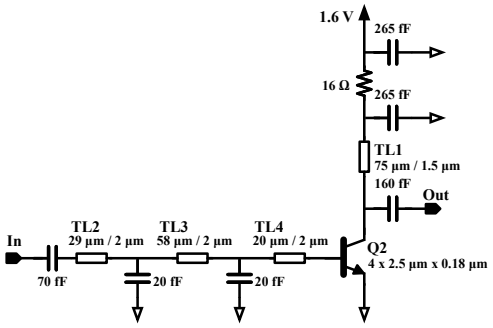


Fig. 5. Schematic of the last stage of the proposed PA.

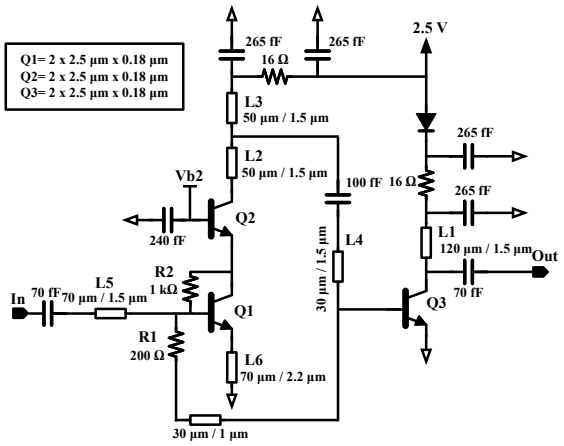


Fig. 6. Schematic of a stage in the proposed LNA.

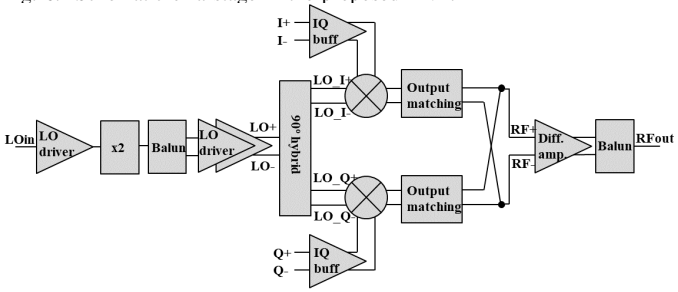


Fig. 7. Block diagram of the D-band quadrature up-converter chip.

between 5 and 6 dB across 140-160 GHz. The core size of this circuit is only 0.16 mm x 0.23 mm.

C. I/Q up- and down-converter

The block diagrams of the IQ modulator and demodulator chips are shown in Fig. 7 and Fig. 8. The same LO chain is used in both chips. It consists of a Marchand balun, a differential LO driver and a differential branch line coupler to generate differential LO signals to drive the quad of the two double balanced mixer (DBM), based on the Gilbert Cell. A frequency doubler is placed at the input, to generate a 140-160-GHz LO signal from a 70-80-GHz input. This doubler is described in Section III-D.

In the demodulator, a Marchand balun generates the differential RF input signal that is fed into input DBM. The output I/Q signals are then buffered by a simple differential pair to get a broadband matching without degrading the overall linearity. As for the modulator, the output of the DBM is matched to 50 Ω and amplified by a differential amplifier before being combined by a Marchand balun to get a single-ended output RF signal. Fig. 9 shows the schematic of the DBM in the up-converter. The output is matched to 50 Ω with a differential T-network.

D. LO frequency multipliers

As mentioned in Section II, an approach consisting of a PLL at lower frequency (X-Band) followed by a frequency multiplication chain, is adopted on this work. The PLL output feeds a frequency multiplier by 6 (sextupler) integrated in a separate chip, as depicted in Fig. 10, which delivers an output

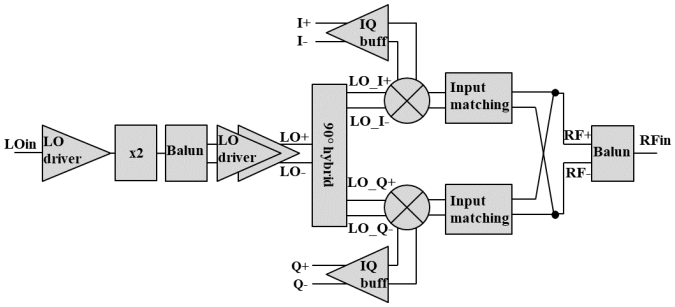


Fig. 8. Block diagram of the D-band quadrature down-converter chip.

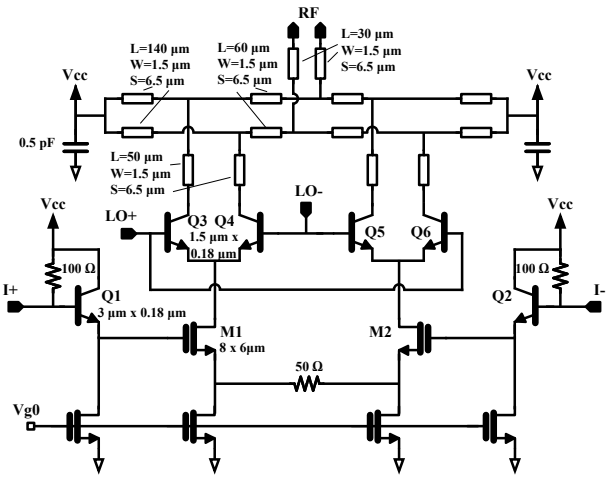


Fig. 9. Schematic of the double balanced up-converter mixer.

signal in the E-band. Then, a frequency doubler, integrated into the up/down converter chip, rises the LO frequency to D-band. This overall multiplication chain architecture, split in two different chips, minimizes design risks and increases testing and debugging flexibility.

The sextupler features high spur rejection, wide bandwidth and low power consumption. As shown in Fig. 10, it is composed of a frequency tripler and a doubler. The schematic of the proposed tripler is depicted in Fig. 11. It takes advantage of a novel circuit topology to reproduce the trans-characteristic of a 3rd order polynomial that ideally generates only the 3rd harmonic of a sinusoidal input signal. More details have been reported in [25].

The schematics of the E-band doubler and the output buffer are shown in Fig. 12. The proposed doubler is based on a push-push transistor pair, Q5-6, but produces a differential output current thanks to C4 and the common-base buffer, Q7. Compared to the widespread push-push doublers [26]–[28], the proposed solution provides a differential output and an enhanced robustness to amplitude and phase imbalance of the driving signal and excellent odd-order harmonic rejection [29].

The D-band doubler, integrated into the I/Q up and down converter chips, has been implemented using the schematic depicted in Fig. 13. The circuit comprises a push-push pair, Q1-Q2, for second harmonic generation, and a stacked common-collector Colpitts oscillator, Q3, which works as a common-base injection-locked amplifier to boost the conversion gain and output power. Standalone test results of the D-band frequency doubler [30] show that the output

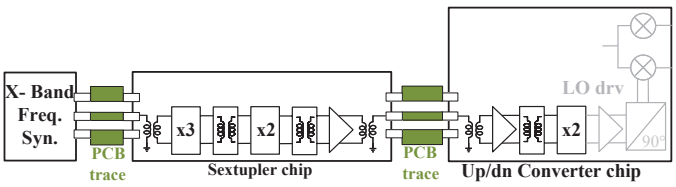


Fig. 10. Top level architecture of the LO chain.

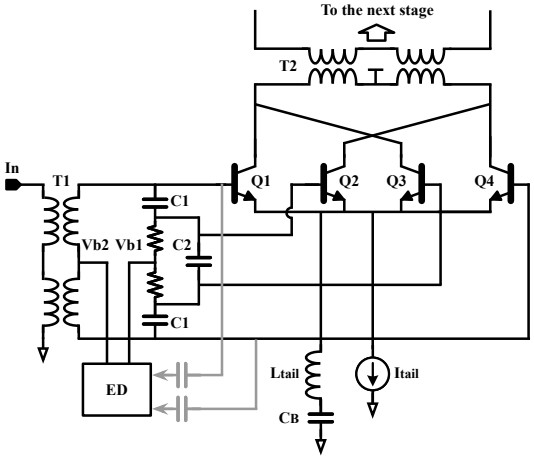


Fig. 11. Schematic of the proposed tripler.

power peaks to 8.1 dBm at 130 GHz, with a conversion gain of 13.1 dB. The output power is maintained above 0 dBm from 108 GHz to 155 GHz, corresponding to a fractional bandwidth of 35.7%. The leakage of the fundamental component is better than 32 dB below the desired signal.

IV. On-wafer test results

A. Test setup

The chips have been fabricated using a 55-nm BiCMOS process provided by STMicroelectronics. Fig. 14 shows pictures of the complete chipset for the proposed D-band phased-array transceiver, including sizes. As observed, the most size-critical blocks, the 4-channel TX and RX antenna array drivers, occupy 1.76 mm x 1.57 mm, which allows their placement within a 4-antenna subarray with a pitch of 1 mm

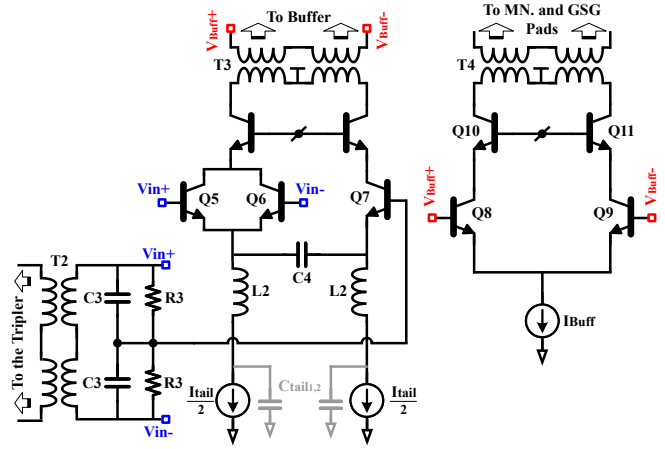


Fig. 12. Schematics of the proposed doubler and the output buffer of the sextupler.

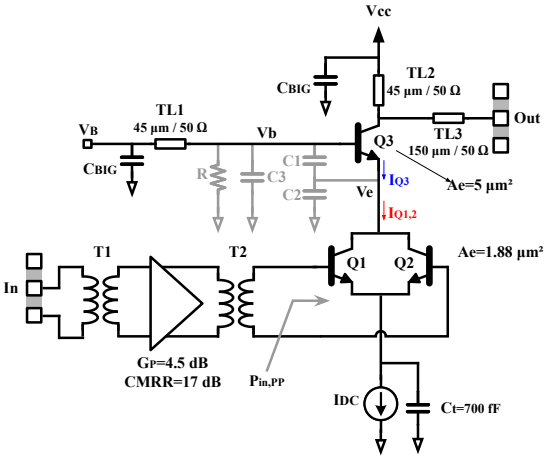
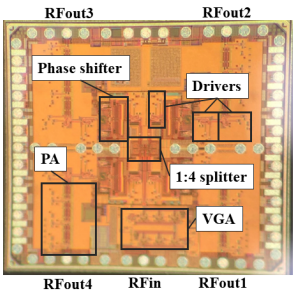
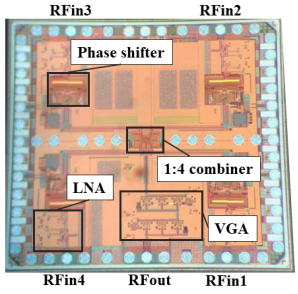


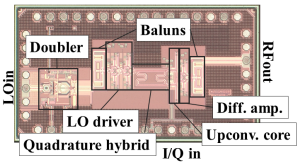
Fig. 13. Schematic of the proposed D-band frequency doubler.



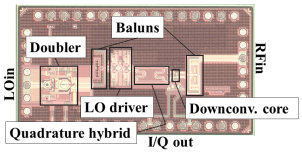
(a) 4-channel TX antenna driver. Size: 1.76 mm x 1.57 mm.



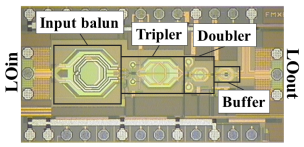
(b) 4-channel RX antenna driver. Size: 1.76 mm x 1.57 mm.



(c) I/Q up-converter. Size: 1.98 mm x 1.08 mm.



(d) I/Q down-converter. Size: 1.98 mm x 1.08 mm.



(e) Frequency sextupler. Size: 1.71 mm x 0.81 mm.

Fig. 14. Pictures of all the implemented chips for the phased-array transceiver.

(λ/2 at 150 GHz).

The chips have been individually characterized before being embedded into the complete transceiver platform. For this purpose, they have been attached to test PCBs. The DC and control signals are provided through wire bonds, while on-wafer probes are used for the RF signals. A BeagleBone Black single-board computer is used to manage the SPI interface of the ICs.

B. Test results

The test results of the 4-channel transmitter chip are summarized in Fig. 15. The gain and phase shift of a TX channel at 150 GHz are shown in Fig. 15 (a), measured

automatically using Keysight Vee to manage both the ICs (through the BeagleBone) and the laboratory equipment. As observed, a phase shift of 0-360° is achievable, with a maximum power gain of around 15 dB at some quadrants. A codebook is generated with all the measured points, so that it is then possible to synthesize any given gain and phase configuration. To check the codebook, sample points with a constant gain of 10 dB and step of 10° are generated and plotted in Fig. 15 (b). The set of measured S-parameters corresponding to one of these 10-dB gain configurations is depicted in Fig. 15 (c). As observed, the bandwidth spans from 130 to 158 GHz, which means a relative bandwidth of 19%. The input and output reflection coefficients are better than -12 dB and -8 dB, respectively, from 130 to 170 GHz. Regarding the large-signal performance, Fig. 15 (d) depicts the measured Pout vs. Pin and Gain vs. Pin curves at 150 GHz, for the same reference configuration. The measured OP1dB is -3.2 dBm, while the saturated output power is bigger than 0 dBm. This measured output power value is smaller than the one measured for the standalone circuits, mainly for two reasons. On the one hand, the integrated 4-channel transmitter suffers more self-heating than the single-ended PA. This can be explained by the fact that the TX chip includes more active blocks and consumes a higher DC power. Moreover, the single-ended PA die is directly placed on the metallic chuck of the on-wafer probe station for its characterization, which helps dissipating the heat better than the PCB used to support the transmitter chip. The hypothesis was verified by blowing some air with a fan over the TX chip during the measurements, which helped improving its performance. Unfortunately, the fan could not be placed close enough due to setup restrictions, and the optimum cooling conditions could not be used for the characterization. On the other hand, wire-bonds are used for the Vcc and ground connections on the chip periphery pads, while the inner ground pads (see Fig. 14(a)) are left unconnected not to interfere with the RF probes. This means that the Vcc and ground connections introduce a non-negligible parasitic inductance that can also affect the performance of the PA, as it employs a single-ended architecture. These issues will be minimized when the chips are assembled in an integration platform, with a dedicated cooling system and higher number of less inductive ground and Vcc connections. The DC power consumption of the 4-channel TX chip is 1.1 W.

Fig. 16 summarizes the measured performance of the 4-channel receiver chip. As in the case of the transmitter, a big number of phase shifter configurations are tested, obtaining the results depicted in the polar plot of Fig. 16 (a), for a frequency of 150 GHz. In this case, a gain of at least 4 dB can be obtained per channel at any output quadrant, while a maximum gain of around 8 dB is exhibited at some points. The measured S-parameters for a reference 4-dB gain configuration are shown in Fig. 16 (b). In this case, the 3-dB bandwidth is 139-160 GHz (13% relative bandwidth). The measured large-signal performance of a receiver channel at 150 GHz is depicted in Fig. 15 (c). The measured IP1dB is -10.4 dBm. As for the noise, Fig. 16 (d) shows the measured and simulated noise figure (NF) of a receiver chain. A minimum noise figure of 15.6 dB is exhibited at 147 GHz, with a value lower than 20 dB from 141 to 161 GHz. The DC power consumption of the 4-channel receiver chip is 0.725 W.

As for the IQ up-converter, the I/Q signals for its characterization are generated using a single generator, a 90° coupler and two baluns. The chip exhibits a broadband response in the range of 130-160 GHz (more than 20% fractional bandwidth), as shown in Fig. 17 (a). For an LO power of -5dBm and a total baseband input power of -1.5 dBm at 20 MHz, the measured CG is around -13.5 dB at 150 GHz with and image rejection ratio (IRR) better than 22 dB and a leaked LO signal of -30 dBm. It should be noted that these results include the effect of the coupler and baluns used in the testbench. In the same conditions, the measured third order intermodulation product (IM3) at 150 GHz is -42 dBc, resulting in an output third order intercept point (OIP3) of 5 dBm. The high linearity of the modulator can also be observed in the gain compression curves of Fig. 17 (b). The input P1dB is better than 7 dBm from 129 to 159 GHz, giving an output power at 1-dB compression between -6 dBm and -3 dBm. Furthermore, the measured 1-dB bandwidth in baseband is greater than 1.3 GHz, which allows using the modulator with channels of up to 2 GHz.

The measured performance of the IQ down-converter is shown in Fig. 18. As observed, it demonstrates a conversion gain around 0 dB from 136 to 162 GHz (18% fractional bandwidth), with an IRR better than 25 dB from 140 to 160 GHz. It exhibits an IP1dB better than 0 dBm, as derived from Fig. 18 (b).

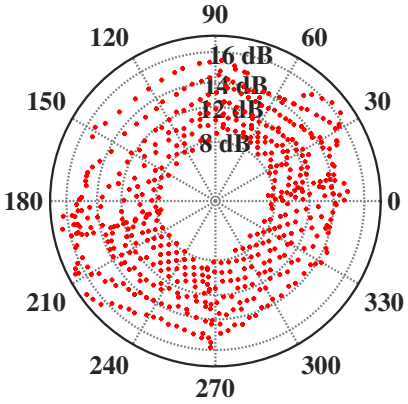
With regard to the tests of the frequency multiplier chip (sextupler), Fig. 19 shows the measured power delivered by the circuit to a 50-Ω load at $6xf_0$ and the leakage of other unwanted harmonics of f_0 versus frequency for a 0-dBm input signal. The measured power consumption is 63 mW. It is observed that the sextupler delivers a peak output power, P_{out}, of 5.6 dBm at 72 GHz, corresponding to a power conversion efficiency of 5.6%. The main tone at $6xf_0$ remains above 0 dBm from 64.7 GHz to 84.7 GHz, corresponding to a 26.8% bandwidth, where the suppression of unwanted harmonics is maintained above 35 dB.

V. Antenna array and integration platform

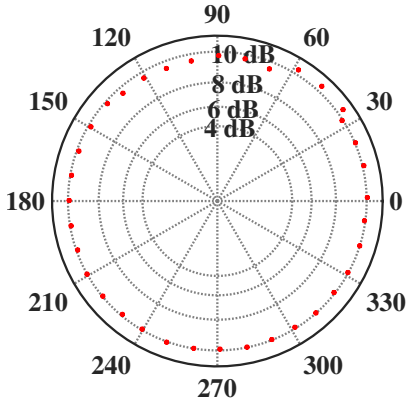
An overview of the integration platform proposed in this work is shown in Fig. 20. A single high-frequency multilayer PCB holds the implemented TX and RX ICs, which are flip-chipped on one layer (L1, or bottom). The same bottom layer is used for the interconnections. The other side (L4, or top) is used for the radiating TX and RX antenna arrays. The PCB assembly with the entire transceiver lays on a heatsink, to dissipate the generated heat. The key elements and processes involved in the proposed integration platform are described in detail below.

A. High-frequency multilayer PCB platform

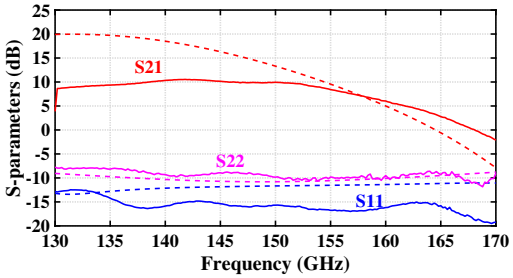
A state-of-the-art PCB technology is chosen for the integration platform of this work. It is based on a 4-layer printed-circuit board (PCB), shown in Fig. 20(b). Megtron 7N ($\varepsilon_r = 3.20$, $tan\delta = 0.003$ at 50 GHz) by Panasonic



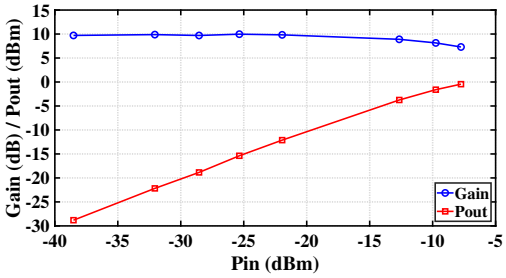
(a) Polar plot with all the measured points at 150 GHz.



(b) Polar plot with all selected points in a 10-dB circle.

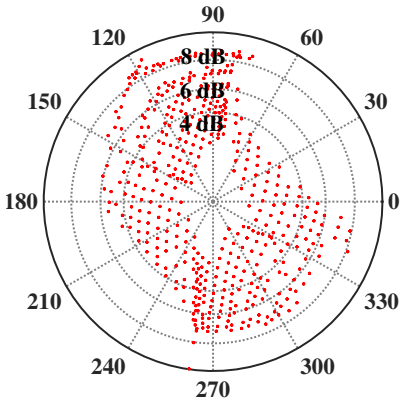


(c) Simulated (dashed) and measured (solid) S-parameters.

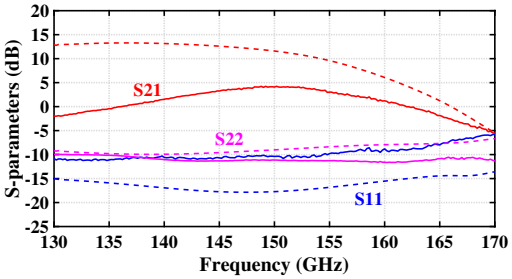


(d) Measured Gain and Pout vs. Pin.

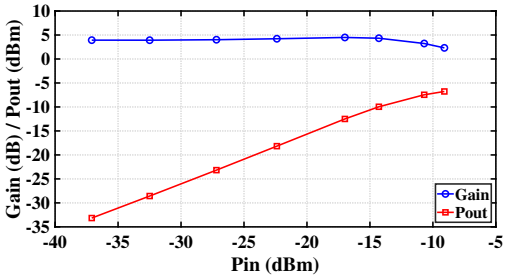
Fig. 15. Test results of a channel in the TX antenna driver chip.



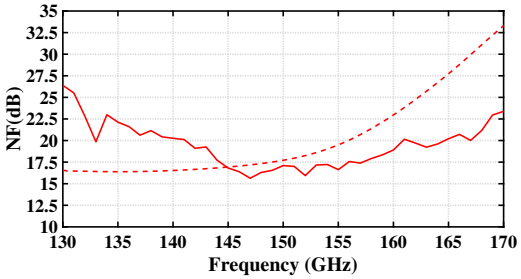
(a) Polar plot with all the measured points at 150 GHz.



(b) Simulated (dashed) and measured (solid) S-parameters.

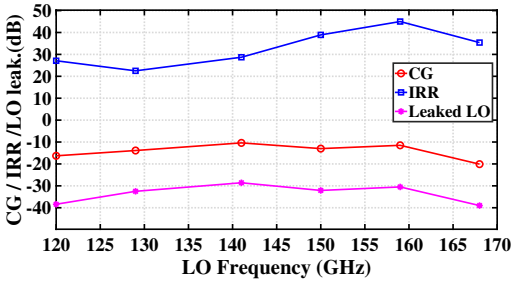


(c) Measured Gain and Pout vs. Pin.

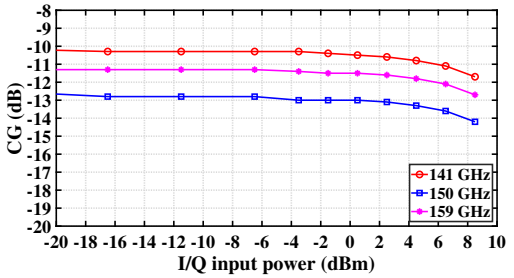


(d) Simulated (dashed) and measured (solid) noise figure.

Fig. 16. Test results of a channel in the RX antenna driver chip.

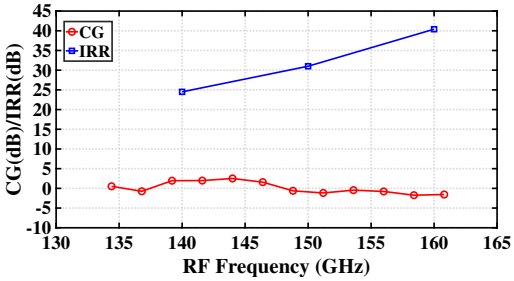


(a) CG, IRR and LO leakage vs. LO frequency, for IF frequency of 20 MHz.

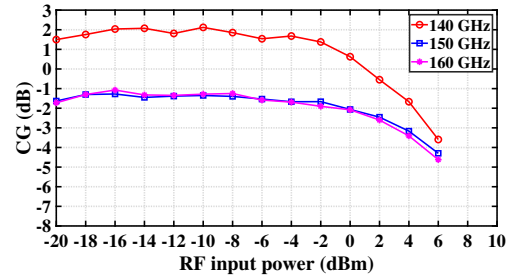


(b) CG vs. I/Q Pin, input quadrature signals at 20 MHz.

Fig. 17. Test results of the IQ up-converter chip.



(a) CG and IRR for the lower sideband vs. RF frequency at 20-MHz IF.



(b) CG vs. RF Pin at 20-MHz IF.

Fig. 18. Test results of the IQ down-converter chip.

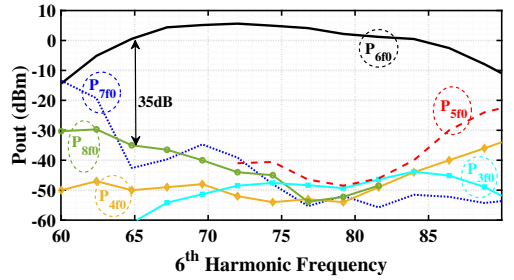


Fig. 19. Measured output power of the 6th harmonic and the largest spureous tones versus frequency for a 0-dBm input signal.

[31] is chosen as substrate material due to its dielectric properties, thickness availability and ease of processing. The total thickness of the PCB is 373 μm, including the plated copper layers. Laser vias between thin and thick layers have diameters of 80 and 100 μm, respectively. Non-plated vias are available as well.

The PCB is manufactured using the high-density interconnect (HDI) any-layer technology, which provides minimum line, spacing and laser drill diameters of 40/40/75 μm in the advanced production option [32]. This feature size is achieved by mSAP (semi-additive processing) on outer copper layers. In mSAP, a thin seed copper layer is coated onto the laminate and plated in the areas where the resist is not applied. Then the seed copper layer between conductors is etched away. The traces are formed with much better accuracy having straight vertical shapes instead of trapezoidal ones of the subtractive process [33]. The distance between ground vias is kept at around 50 μm in critical areas, to fulfill the rule of thumb of keeping the distance smaller than $\lambda/20$. Test structures of the antenna array elements and interconnection structures exhibit very good manufacturing accuracy, being the realized patch dimensions only 2.5% smaller than the designed ones [34]. The platform has demonstrated good interconnection performance in D-band. The measured losses for a microstrip line and a coplanar waveguide at 150 GHz are 1.9 dB/cm and 1.8 dB/cm, respectively, while flip-chip transitions to these lines feature a measured loss of 0.3 dB for 60-μm bumps [35]. Microstrip lines in L1, with ground in L2, are used to implement the 4-way dividers connecting the IQ modulator/demodulator with the antenna driver chips. Due to unavailability of discrete isolation resistors valid for D-band frequencies, T-type dividers are implemented, with the subsequent lack of isolation between outputs. Based on the aforementioned measurements of a microstrip line in this PCB substrate, the insertion loss of the dividers is estimated to be 0.6 dB on top of the 6 dB due to 4-way power splitting.

The transition between the ICs and the PCB with the antennas is critical at D-band frequencies. In particular,the height of the connection and the consequent chip-PCB spacing have a strong impact on the impedance presented to the chip ports, the antenna radiation pattern and the input-output isolation in the chips. EM simulation results of a 2x2 antenna sub-array connected to a 4-channel IC are depicted in Fig.21. The picture shows the reflection coefficient at the chip output ports and the maximum array gain at 150 GHz as a function of the connection height. As observed, a height bigger than 80 μm is required for optimum performance. This result is consistent with the fact that, as microstrip lines in L1-L2 with a substrate height of 64 μm are employed for the antenna feeding lines, the silicon chips disturb the field distribution of the lines when placed in close proximity. The required connection height can be achieved with a Cu-pillar based attachment process, where the pillar height can be accurately controlled.

The ICs described in Section III are processed in a multi-project wafer and are only available as separate dies, while entire wafers are needed for Cu-pillar growing. Alternatively, solder bumps can be processed on these ICs

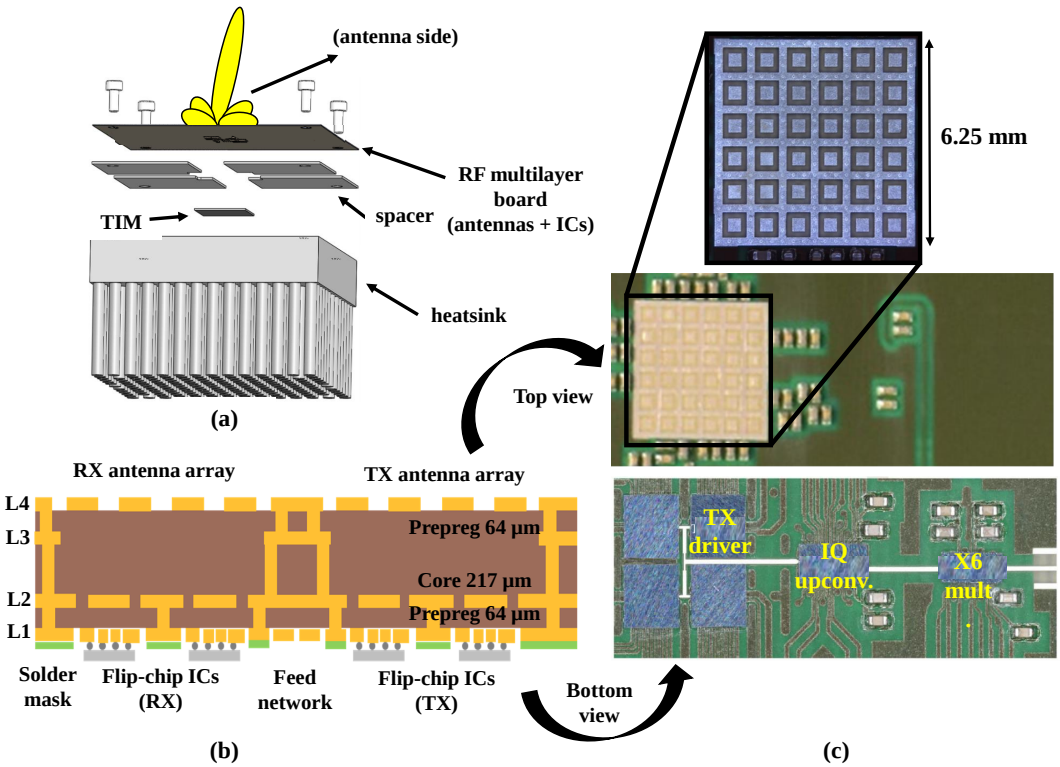


Fig. 20. Proposed integration platform.

using solder jetting and laser reflow. In this case, the diameter of the spherical solder balls needs to be compatible with the chip pad dimensions. A solder ball size of 60 μm is chosen for this work, a value that balances the trade off between connection height and the parasitic capacitance associated to big chip pads. The solder alloy is SAC305. Prior to adding the solder balls, the aluminum contact pads on the dies are gold plated in a separate process step. An advanced laser-assisted bonding (LAB) technology is used for flip-assembly of the dies on the PCB [36]. A ~25-μm thin solder mask around the PCB contact pads prevents the solder from flowing along the copper tracks.

Fig. 20(c) shows part of the assembled transceiver, particularly the TX chain, consisting of the x6 multiplier chip (right), IQ modulator (center) and 4 TX antenna driver chips (left). After the assembly, the bump size was inspectioned, observing that their final height was around 30 μm. This height is smaller the original 60-μm diameter, as compression of solder balls always happens in a reflow process. As derived from Fig. 21, this small 30-μm bump size will negatively impact the performance of the system, with a S11 of around -3 dB and an array gain 4 dB below its maximum. Moreover, the poor impedance matching at the chip ports can severely impact the performance of the implemented single-ended circuits. To improve this situation, solder ball stacking in order to increase the final bump height was tried but was not successful. In any case, even if the performance will be not the optimum, the assembly is completed and good enough to prove the validity of other aspects of the phased-array platform, such as the chipset, PCB and antenna designs and 2D beam-steering

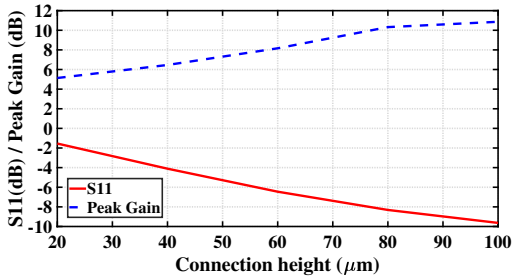


Fig. 21. Simulated effect of the bump height on the antenna array performance at 150 GHz.

functionality, among others. In wafer-scale production, the solder bumps will be replaced by copper pillars of required height and these effects would be alleviated, moving the performance closer to its optimum.

B. 16-element phased antenna array

A 16-element planar antenna array is designed for the transmitter and the receiver proposed in this work. The antenna element separation is 1 mm ($\lambda_0/2$), which enables the maximum scanning range for the phased array. Dummy antennas, unconnected to the circuitry, are placed in the periphery to ensure a symmetrical surrounding and thus a more similar radiation pattern for all the active antenna elements. The total size of the array, including the dummy antennas, is 6.25 mm x 6.25 mm. All the RF, DC and control interconnects must fit into the spacing between chips, which imposes tight area restrictions to the chips as introduced in Section II.

A picture of the antenna array is shown in Fig. 20(c). A cavity-backed aperture-coupled patch antenna topology is chosen in this work. Its main advantage is the reduction of surface-wave power, especially in the E-plane [37], [38], which results in an enlarged scanning range in the phased array [39]. To further improve the isolation between antenna elements in the E-plane, via fences are constructed over the horizontal center line of the TX and RX chips, where ground pads are placed with a separation smaller than $\lambda/20$ (see Fig. 14).

The antenna array is designed for an operating frequency range of 140-160 GHz (20%), which requires the use of wideband antenna elements. Each antenna element is fed using a microstrip line on L1, according to the stack-up shown in Fig. 20(b), while the patch on L4 is excited through a coupling aperture in the ground plane on L2. The measured maximum gain for the 16-element antenna array is 14 dBi at 143 GHz, while the measured antenna input matching bandwidth is 20 GHz. More details about the antenna array design and characterization are presented in [34]. With this measured antenna array gain, a maximum EIRP of 26 dBm would be achievable with the measured 0-dBm Psat at the output of each TX chain.

C. Complete TX/RX demonstrator unit

The complete constructed test bench for the D-band radio link tests is shown in Fig. 22. The prototype is assembled on a chassis made of a durable Delrin plastic material. As the implemented active antenna array chips generate a lot of heat in a small area ($\sim$0.4 W/mm^2), a cooling system consisting of a heat sink with forced convection (fan) is used. The heat sink supports the PCB on top of it and contacts the chips through a thermal interface material (TIM), as observed in Fig. 20(a).

In addition to the RF and antenna boards described earlier, there are multiple auxiliary electronic boards. These include two ADF4372 evaluation boards with independent integrated frequency references, for the X-band LOs; a Beagle Bone Black single board computer (SBC) to control the SPI and manage the beam forming; custom modem boards with low-pass filters and level control; interface boards with baseband amplifiers (AD LTC6409) and DC/DC converters for the power supply.

VI. Over-the-air tests

The 16-element phased array transceiver unit described in Section V is characterized over the air in a laboratory environment (the demo video is available in [40]). The DC power consumed by all the employed ICs is summarized in Table I. Under these operation conditions, with both the TX and RX on, pictures obtained with a thermal camera show a temperature below 40°C at the chip surfaces, which demonstrates the correct operation of the implemented heat management system.

Firstly, beam steering is demonstrated using a manually operated rotational table. The phased array under test is scanned between $\pm 40°$, while the radiation patterns are recorded between $\pm 50°$ in 5° steps. For these tests, the codebooks generated during the on-wafer characterization

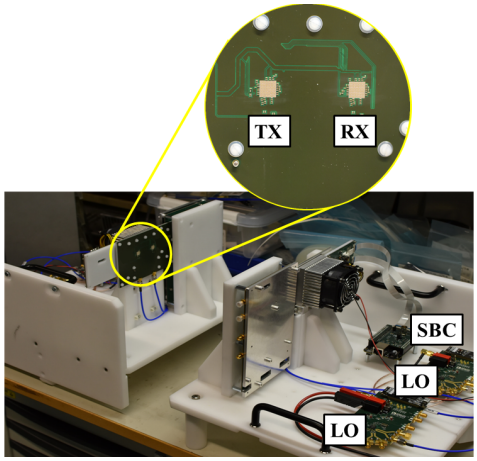


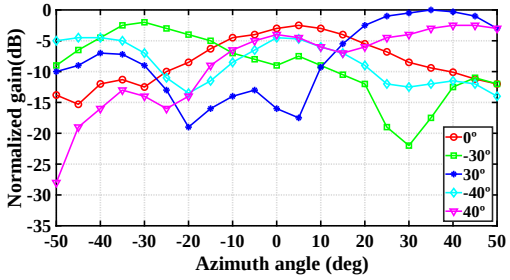
Fig. 22. Test bench for the D-band demo link trials.

TABLE I
DC power breakdown for the 16-element phased array transceiver.

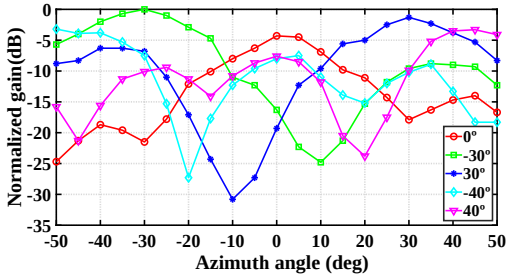
Element	TX	RX
Antenna driver	4 x 1.1 W	4 x 0.725 W
IQ up/down converter	0.4 W	0.42 W
x 6 LO multiplier	63 mW	63 mW
Total	**4.86 W**	**3.38 W**

described in Subsection IV-B are used. The results for the transmitter and receiver are shown in Fig. 23, for frequencies of 145 and 152 GHz, respectively. It can be observed that the main beam is steered in the azimuth plane towards the predefined angles. The results show that the phased array proposed in this work is operational and works as expected.

More accurate radiation patterns of the receiver are determined by a planar near-field measurement, where an open-ended waveguide probe connected to a VDI WR-5.1 VNA extender is used as the transmitter. The scanning distance and area



(a) Transmitter.



(b) Receiver.

Fig. 23. Manually measured radiation patterns at 17 cm.

are 9 cm and 32 cm x 32 cm, respectively. That scanning area enables near field to far field transformation up to $\pm 60^\circ$ in azimuth and elevation. Absorbers are used both in the phased antenna array under test and around the near-field probe antenna to reduce reflections. Antenna aperture filtering is utilized to avoid the effects of reflections from the support structures and the small radiation leakage from the waveguide flange observed in the measured radiation patterns. More details about the measurement procedure are detailed in [34].

The radiation patterns are measured for different cases: broadside, $\pm 30^\circ$ beam steering in azimuth, diagonal and elevation planes, -40° in azimuth plane and cross-polarized pattern for broadside. The measured radiation patterns at 150 GHz are shown in Fig. 24. It can be observed that the main lobe, shown in red, is steered to the predefined angles. Side lobes are also visible in the patterns, with a maximum level of about -5 dB. These patterns prove the functionality of the proposed phased array system, demonstrating that the beam can be steered at least $\pm 30^\circ$ in azimuth and elevation planes (2D) and up to even -40° in the azimuth plane. The scanning range in the measurements was limited up to $\pm 60^\circ$ due to scanning time constraints. The last plot shows the cross-polarized pattern for the broadside direction. The cross-polarization level is about -18 dB at maximum, which is quite acceptable for a phased antenna array. The power level at the maximum is mostly within 7 dB range for all the tested beams. Both the side-lobe level and the power level variation could be reduced with array calibration and codebook optimization, as the codebooks extracted from on-wafer measurements were used for the presented tests, without taking into account the effect of the assembly structure. In addition, the plastic mechanics may block some of the radiation at large angles. The same measurements have been taken at 140 and 160 GHz as well, observing a similar behavior.

A bi-directional D-band radio link is also demonstrated in the laboratory. Firstly, a test is performed with tones, separating the radio units by a distance of 34 cm. For that, the transmitter LO is programmed at 150 GHz, with the I/Q signals at 100 MHz with amplitudes of -6 dBm, while the receiver LO is set at 149.8 GHz. These frequencies can be set as desired, as long as both sides of the radio link are set up adequately. The received signal, after down-conversion, is shown in Fig. 25(a). As observed, the image rejection is around 20 dB and the leaked LO is more than 25 dBc below the main tone at 300 MHz. Secondly, a test is performed with QPSK-modulated signals, using custom modem units. The radio frequencies are set so that the first TX-RX pair operates at 156 GHz and the second TX-RX pair operates at 150 GHz. The measured constellation for a 62.5-MHz channel (52 Mbaud) is shown in Fig. 25(b).

Test bandwidth and modulation order were limited by the less-than-expected height of the flip-chip connections, as discussed in Section V. These introduce lower array gains, extra ripples and worse performance of the PA and LNA due to their high sensibility to the impedance mismatch. In addition, the close proximity between the chip and the PCB together with the reflections at the PA port make it necessary to back-off the transmitter gain to avoid stability problems.

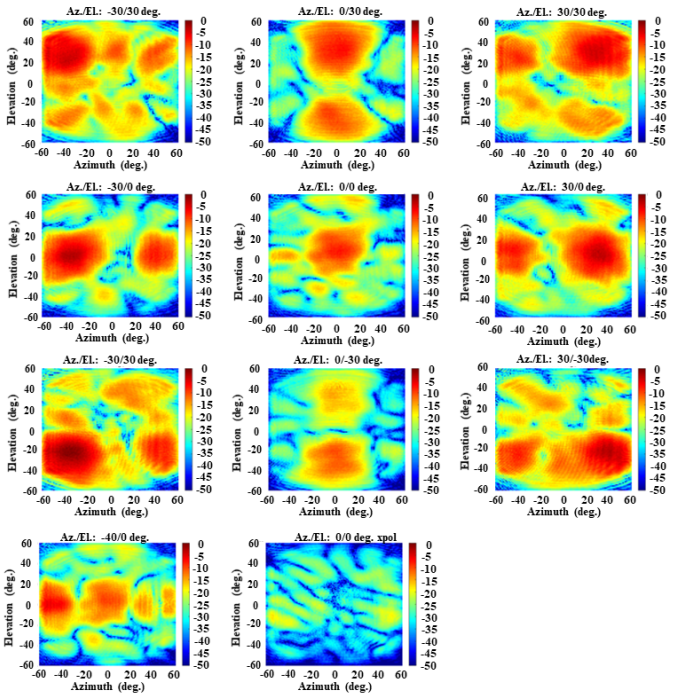


Fig. 24. Measured radiation patterns of the receiver at 150 GHz.

The measured performance of the complete 16-element D-band phased array transceiver is summarized in Table II, together with other experimentally demonstrated mm-wave phased array systems. As observed, the exhibited performance is comparable to that of systems operating at similar and lower frequencies. The presented work features 16 TX/RX chains per array and incorporates 4 chains in a compact die. This compactness implies a penalty in features like the output power, but in turn allows addressing each antenna element in the phased array independently and thus enables beam steering capabilities in both azimuth and elevation.

Both the wide RF bandwidth of the presented chipset and the fact that the communication link can be placed anywhere in the 140-160 GHz band prove that the presented phased array transceiver is suitable for fFDD communication schemes.

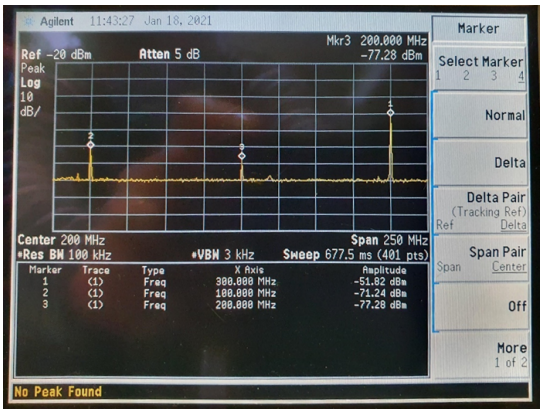
VII. Conclusion

A complete 16-element D-band phased array transceiver with 2D beam steering functionality, suitable for the next generation of front and backhaul radio links, has been presented in this work. The chipset is integrated using a 55-nm SiGe BiCMOS process, demonstrating that commercially available low-cost silicon-based processes can be used for the implementation of fully functional D-band systems on chip. 4-channel compact TX and RX chips are implemented. The proposed approach facilitates driving each antenna element independently, thus enabling wideband and frequency-independent beam steering in the azimuth and elevation planes. Both the bidirectional beam-steering functionality and a complete radio link are demonstrated over the air, for the first time at D-band, to the best of the authors' knowledge.

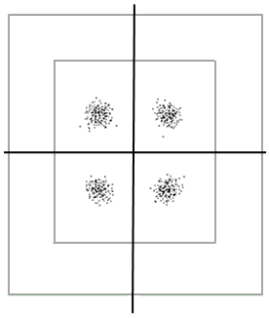
TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART IN CMOS AND BICMOS TECHNOLOGIES.

Ref.	Tech.	Fc (GHz)	RX NF (dB)	TX Psat (dBm)	RX Pdc (W)	TX Pdc (W)	antennas/ array	TX-RX chains/ array	Peak EIRP (dBm)	chains/ chip	Level of integration
[8]	120-nm BiCMOS	60	6.8	–	1.8	–	16	16	–	16	LNA, phase shifter, combiners, LO mult. and buffers, VGAs, I/Q downconv.
[9]	180-nm BiCMOS	60	–	3	–	8 / 32	64/256	64/256	38 / 45	64	PA, phase shifter, splitters, VGA, antennas
[41]	130-nm BiCMOS	94	12.5	6.4	0.364**	0.364**	4	4	20	4 TX + 4 RX	LNA, PA, phase shifter, VCO, LO mult. and buffers, splitters
[42]	180-nm BiCMOS	94	6.5	8	4.5**	5.5**	16	16	34	16 TX + 4 RX	LNA, PA, phase shifter, PLL, combiners, splitters, I/Q up and downconv, self-test, analog base-band
[10]	180-nm BiCMOS	94	6.5	8	57.6**	70.4**	256	256	60	16 TX + 4 RX	LNA, PA, phase shifter, PLL, combiners, splitters, I/Q up and downconv, self-test, analog base-band
[11]	65-nm CMOS	140	11*	4*	0.92		4	2	N.A.	1	LNA, PA, phase shifter, LO mult. and buffers, IF upconv.
[13]	130-nm BiCMOS	150	10	13	2.64**	5.28**	128	8	N.A.	1	LNA, PA, phase shifter
This work	**55-nm BiCMOS**	**150**	**15.6**	**0**	**3.4**	**4.9**	**16**	**16**	**26****	**4**	**LNA, PA, phase shifter, VGA, combiners, splitters, LO mult. and buffers, I/Q up. and downconv.**

*Simulation result. **Estimated from DC power of unitary chain. *** Calculated from Psat and antenna array gain.



(a) Received tones.



(b) Received constellation.

Fig. 25. Measurements of the complete radio link in the laboratory.

The key aspects of the integration of this kind of D-band phased array transceivers have been deeply described, identifying the main challenges. The system is assembled in a commercial PCB platform, employing HDI and mSAP technologies. PCB-to-chip separation is a critical aspect in this kind of integration platform. The suggested roadmap includes growing, at wafer-scale, copper pillars of controlled height over the chip pads, as well as implementing antenna feeding structures less sensitive to the presence of the silicon chips.

Although the size restrictions for the antenna driver chip and the proximity to the f_T of the technology limit the output power and pose demanding requirements to the thermal management, this will be alleviated by next generation of BiCMOS technologies.

ACKNOWLEDGMENT

The authors would like to thank Mr Ismo Huhtinen, Dr Mikko Kantanen and Mr Alpo Ahonen for their support in the measurements. Dr Juha Ala-Laurinaho from Aalto University is acknowledged for the near-field measurements and pattern data processing.

REFERENCES

[1] P.-H. Kuo and A. Mourad, "Millimeter Wave for 5G Mobile Fronthaul and Backhaul," in *2017 European Conference on Networks and Communications (EuCNC)*, 2017, pp. 1–5.

[2] Y. Li and J. Hansryd, "Fixed Wireless Communication Links Beyond 100 GHz," in *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 31–33.

[3] *Radio frequency channel/block arrangements for Fixed Service systems operating in the bands 130-134 GHz, 141-148.5 GHz, 151.5-164 GHz and 167-174.8 GHz*, ECC ECC Recommendation (18)01, 2018.

[4] M. G. L. Frecassetti *et al.*, "D-Band Radio Solutions For Beyond 5G Reconfigurable Meshed Cellular Networks," in *2019 16th International Symposium on Wireless Communication Systems (ISWCS)*, 2019, pp. 427–431.

[5] A. Pallotta *et al.*, "SiGe:BiCMOS technology is enabling D-band link with Active Phased Antenna Array," in *2021 Joint European Conference on Networks and Communications 6G Summit (EuCNC/6G Summit)*, 2021, pp. 496–501.

[6] M. Wietstruck, S. Marschmeyer, S. Schulze, S. T. Wipf, C. Wipf, and M. Kaynak, "Recent Developments on SiGe BiCMOS Technologies for mm-wave and THz Applications," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 1126–1129.

[7] B. Sadhu, X. Gu, and A. Valdes-Garcia, "The More (Antennas), the Merrier: A Survey of Silicon-Based mm-Wave Phased Arrays Using Multi-IC Scaling," *IEEE Microwave Magazine*, vol. 20, no. 12, pp. 32–50, Dec 2019.

[8] A. Natarajan *et al.*, "A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, 2011.

[9] S. Zihir, O. D. Gurbuz, A. Kar-Roy, S. Raman, and G. M. Rebeiz, "60-GHz 64- and 256-Elements Wafer-Scale Phased-Array Transmitters Using Full-Reticle and Subreticle Stitching Techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4701–4719, 2016.

[10] S. Shahramian, M. J. Holyoak, A. Singh, and Y. Baeyens, "A Fully Integrated 384-Element, 16-Tile, W-Band Phased Array With Self-Alignment and Self-Test," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2419–2434, 2019.

[11] S. Ma, J. Lin, C. Ma, and H. Yu, "A 140 GHz Transceiver for 4x4 Beamforming Short-Range Communication in 65nm CMOS," in *2019 IEEE Asia-Pacific Microwave Conference (APMC)*, 2019, pp. 1613–1615.

[12] A. Hamani *et al.*, "An 84.48 Gb/s CMOS D-band Multi-Channel TX System-in-Package," in *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021, pp. 207–210.

[13] M. Elkhouly *et al.*, "D-band Phased-Array TX and RX Front Ends Utilizing Radio-on-Glass Technology," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 91–94.

[14] M. Elkhouly *et al.*, "Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules," in *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 76–78.

[15] M. G. L. Frecassetti, A. Mazzanti, J. F. Sevillano, D. del Rio, and V. Ermolov, "D-Band Transport Solution to 5G and Beyond 5G Cellular Networks," in *2019 European Conference on Networks and Communications (EuCNC)*, 2019, pp. 214–218.

[16] *Point-to-Point Radio Links in the Frequency Ranges 92-114.25 GHz and 130-174.8 GHz*, ECC Report 282, 2018.

[17] M. Fakharzadeh, M. Nezhad-Ahmadi, B. Biglarbegian, J. Ahmadi-Shokouh, and S. Safavi-Naeini, "CMOS Phased Array Transceiver Technology for 60 GHz Wireless Applications," *IEEE Transactions on Antennas and Propagation*, vol. 58, no. 4, pp. 1093–1104, April 2010.

[18] D. del Rio, A. Irizar, I. Gurutzeaga, A. Rezola, R. Berenguer, and J. F. Sevillano, "Design of Integrated Control Circuits for mm-Wave Phased Arrays in 55-nm BiCMOS," in *2019 XXXIV Conference on Design of Circuits and Integrated Systems (DCIS)*, 2019, pp. 1–5.

[19] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," in *2014 IEEE International Electron Devices Meeting*, 2014, pp. 3.9.1–3.9.3.

[20] P. Roux, A. Singh, F. Jorge, M. Moretto, and Y. Baeyens, "Wideband Variable Gain Amplifier for D-band Backhaul Transceiver in 55nm BiCMOS Technology," in *2019 IEEE Asia-Pacific Microwave Conference (APMC)*, 2019, pp. 1313–1315.

[21] P. V. Testa, C. Carta, and F. Ellinger, "A 160-190-GHz Vector-Modulator Phase Shifter for Low-Power Applications," *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 1, pp. 86–89, 2020.

[22] Y. Kim, S. Kim, I. Lee, M. Urteaga, and S. Jeon, "A 220-320-GHz Vector-Sum Phase Shifter Using Single Gilbert-Cell Structure With Lossy Output Matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 1, pp. 256–265, 2015.

[23] M. Kantanen, J. Holmberg, M. Varonen, and A. Rantala, "Digitally controlled vector modulator SiGe MMIC for millimeter-wave phased array applications," in *2018 11th German Microwave Conference (GeMiC)*, 2018, pp. 51–54.

[24] D. del Rio, I. Gurutzeaga, R. Berenguer, I. Huhtinen, and J. F. Sevillano, "A Compact and High-Linearity 140-160 GHz Active Phase Shifter in 55 nm BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 2, pp. 157–160, 2021.

[25] M. M. Pirbazari, F. Pepe, and A. Mazzanti, "40GHz Frequency Tripler with High Fundamental and Harmonics Rejection in 55nm SiGe-BiCMOS," in *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, 2019, pp. 229–232.

[26] Y. Ye, B. Yu, A. Tang, B. Drouin, and Q. J. Gu, "A High Efficiency E-Band CMOS Frequency Doubler With a Compensated Transformer-Based Balun for Matching Enhancement," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 1, pp. 40–42, 2016.

[27] H.-C. Lin and G. M. Rebeiz, "A 135-160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1–4.

[28] I. Lee, Y. Kim, and S. Jeon, "108-316- and 220-290-GHz Ultrabroadband Distributed Frequency Doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 3, pp. 1000–1011, 2020.

[29] M. M. Pirbazari and A. Mazzanti, "E-Band Frequency Sextupler With gt;35 dB Harmonics Rejection Over 20 GHz Bandwidth in 55 nm BiCMOS," *IEEE Journal of Solid-State Circuits*, pp. 1–12, 2022.

[30] M. M. Pirbazari and A. Mazzanti, "High Gain 130-GHz Frequency Doubler With Colpitts Output Buffer Delivering Pout up to 8 dBm with 6% PAE in 55-nm SiGe BiCMOS," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 36–39, 2021.

[31] "Megtron7 Data Sheet," Panasonic. [Online]. Available: https://industrial.panasonic.com/content/data/EM/PDF/ipcdatasheet_R-5785(G).pdf

[32] "HDI any layer PCBs," AT&S, Leoben, Austria. [Online]. Available: https://ats.net/products-technology/product-portfolio/hdi-any-layer-pcbs

[33] M. Gantz, "mSAP: The new PCB manufacturing imperative for 5G smartphones," Orbotech, Yavne, Israel, February 2017. [Online]. Available: https://cdn.baseplatform.io/files/base/ebm/electronicdesign/document/2019/04/electronicdesign_19002_orbotech_pdflayout.pdf

[34] A. Lamminen, J. Säily, J. Ala-Laurinaho, J. de Cos, and V. Ermolov, "Patch Antenna and Antenna Array on Multilayer High-Frequency PCB for D-Band," *IEEE Open Journal of Antennas and Propagation*, vol. 1, pp. 396–403, 2020.

[35] A. Lamminen, M. Lahti, D. del Rio, J. Säily, J. F. Sevillano, and V. Ermolov, "Characterization of Interconnects on Multilayer High Frequency PCB for D-Band," in *2020 2nd 6G Wireless Summit (6G SUMMIT)*, 2020, pp. 1–5.

[36] A. Kolbasow, T. Kubsch, M. Fettke, G. Friedrich, and T. Teutsch, "Vertical Laser Assisted Bonding for Advanced "3.5D" Chip Packaging," in *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, 2019, pp. 210–217.

[37] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. USA: Wiley-Interscience, 2005.

[38] J. Aberle and F. Zavosh, "Analysis of probe-fed circular microstrip patches backed by circular cavities," *Electromagnetics*, vol. 14, no. 2, pp. 239–258, 1994.

[39] F. Zavosh and J. Aberle, "Infinite phased arrays of cavity-backed patches," *IEEE Transactions on Antennas and Propagation*, vol. 42, no. 3, pp. 390–398, 1994.

[40] "D-band Radio solution Enabling up to 100 Gbps reconfigurable Approach for Meshed beyond 5G networks," June 2021. [Online]. Available: https://www.youtube.com/watch?v=Ioaq3a_IboM

[41] A. Townley *et al.*, "A 94-GHz 4TX–4RX Phased-Array FMCW Radar Transceiver With Antenna-in-Package," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1245–1259, 2017.

[42] S. Shahramian, M. J. Holyoak, and Y. Baeyens, "A 16-Element W-Band Phased-Array Transceiver Chipset With Flip-Chip PCB Integrated Antennas for Multi-Gigabit Wireless Data Links," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 7, pp. 3389–3402, 2018.

David del Rio (Member, IEEE) received the M.Sc. and Ph.D. degrees in telecommunication engineering from Tecnun—University of Navarra, Donostia-San Sebastian, in 2013 and 2017, respectively, with a focus on BiCMOS transmitters for Multi-Gbps E-Band communications. In 2016, he was a Visiting Graduate Researcher with the High Speed Electronics Laboratory, University of California at Los Angeles, where he was involved in the design of CMOS integrated transceivers for 5G communications. Dr. del Rio is currently a Researcher with the Electronics Systems and Communications Group in Ceit Research Centre, Donostia-San Sebastian. He is also an Associate Professor with the Electrical and Electronic Engineering Department, Tecnun—University of Navarra. His current research interests include millimeter-wave (mmW) and RF circuit design, power amplifiers, phased arrays and reconfigurable devices for self-healing systems.

Juan F. Sevillano (Senior Member, IEEE) was born in Irun, Basque Country, Spain, in 1975. He received his M. Sc. degree in Electrical, Electronic, and Control Engineering in 1999 and his Ph. D. degree in 2004, both from the University of Navarra, San Sebastian, Spain. In 1999, he was an assistant researcher at the Fraunhofer Institut for Integrated Circuits IIS, Erlangen, Germany, where he was involved in projects related to satellite broadcasting systems. In 2000, he joined CEIT, Research Centre, San Sebastian, Spain, where he is involved in projects related to wireless communications and sensor systems. Since 2001, he is also a lecturer at TECNUN, Technology Campus of the University of Navarra, San Sebastian, Spain. His current research interests are in the area of communication system design and implementation, signal processing and sensor system design and implementation.

Rolando Torres received his bachelor's degree and MSc. degree in electronic engineering from the Universidad Industrial de Santander (UIS), in 2015 and 2019, respectively. During his master thesis he worked in the design of front-end circuits for high-speed interfaces. In 2019, he was invited as a visiting researcher in Tubitak-Bilgem, Gebze, Turkey, where he was part of the radio-frequency design team working on voltage and current reference circuits. He joined the Electronics Systems and Communications Research Group at Ceit in 2021, to start his Ph.D. research on radio frequency circuits for transceivers operating in frequencies above 100 GHz.

Andoni Irizar received his degree in Industrial Engineering from the University of Navarra, San Sebastian (Spain) in 1991 and a doctorate in electrical engineering from the University of Sheffield (UK) in 1998. Since 1996 he is a researcher at Ceit where he is working in the Group of Intelligent Systems for Industry 4.0. He is the author of 25 articles and contributions to international Conferences. His main research interests are the implementation of Digital Signal Processing algorithms for Communications Systems. He has also led National and International Projects (public and privately funded) in OFDM, UWB, DVB-T / T2 and RFID systems. Currently he is working on the development of sensor devices to monitor physical variables and processes for the manufacturing and operation of industrial components.

Pascal Roux (Member, IEEE) received his M.Sc. degree in telecommunications from the university of LIMOGES, France, in 1987 and he joined the R&D department of THALES (former Thomson-CSF) as an R&D engineer, where he designed millimeter wave GaAs IC and RF-heads. In 2000, he joined Nokia Bell Laboratories France (Former Bell laboratories of Lucent Technology) to develop electronic and opto-electronics circuits for terabit optical and wireless applications. He holds 3 patents and has authored or coauthored more than 25 technical articles.

Mahmoud M. Pirbazari (Member, IEEE) received the M.Sc. degree in electrical engineering from Urmia University, Urmia, Iran, in 2014, and the Ph.D. degree in microelectronics from The University of Pavia, Pavia, Italy, in 2020, with a focus on frequency multiplication circuits with outputs at E- to D-band used in high data rate millimeter-wave transceivers. He joined the AIC Laboratory, The University of Pavia, in 2017, as a Researcher, where he started his Ph.D. in the same year. He is currently with the AIC Laboratory, as a Post-Doctoral Researcher working on millimeter-wave circuit building blocks in BiCMOS technology. Dr. Pirbazari was a recipient of the 2020 SSCS Pre-Doctoral Achievements' Award.

Andrea Mazzanti (Senior Member, IEEE) received the Laurea and Ph.D. degrees in electrical engineering from the University of Modena and Reggio Emilia, Modena, Italy, in 2001 and 2005, respectively. During the summer of 2003, he was with Agere Systems, Allentown, PA, USA, as an Intern. From 2006 to 2009, he was an Assistant Professor with the University of Modena and Reggio Emilia. In January 2010, he joined The University of Pavia, Pavia, Italy, where he is currently a Full Professor. He has authored or coauthored more than 100 technical articles. His main research interests cover device modeling and IC design for high-speed communications, RF, and millimeter-wave systems. Dr. Mazzanti has been a member of the Technical Program Committee of the IEEE Custom Integrated Circuit Conference (CICC) from 2008 to 2014, the IEEE European Solid State Circuits Conference (ESSCIRC), and the IEEE International Solid State Circuits Conference (ISSCC) from 2014 to 2018. He has been an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS from 2012 to 2015 and a Guest Editor for special issues of the IEEE JOURNAL OF SOLID-STATE CIRCUITS dedicated to CICC 2013–2014 and ESSCIRC-2015. Since 2017, he has been serving as an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS.

Jussi Säily was born in Rantsila, Finland, in 1974. He received the M.Sc., Lic.Tech., and D.Sc.(Tech.) degrees in electrical engineering from Helsinki University of Technology (TKK), Espoo, Finland, in 1997, 2000, and 2003, respectively. From 1997 to 2003, he was a Research Engineer with the Radio Laboratory, TKK. Since 2004, he has been with VTT where he is a Senior Scientist and Project Manager in the Antennas and RF Technology research group. His research interests include beam steerable mm-wave antenna arrays for 5G and 6G communications, mm-wave lens antennas, mm-wave radar, phased arrays, satellite antennas, advanced low-loss antenna substrates and manufacturing methods, RFID antennas, RF electronics, and phase-locked low-noise signal sources for instrumentation. Dr. Säily holds several patents on communications antennas, and has over 100 publications in international journals and conference proceedings. He serves regularly as a reviewer for technical journals, including IEEE Transactions on Antennas and Propagation, IEEE Antennas and Wireless Propagation Letters, Electronics Letters, and funding agencies like the European Science Foundation. He's also a Finnish national delegate of the COST IC0603 (ASSIST) and COST IC1102 (VISTA) management committees.

Antti Lamminen received the M.Sc. and D.Sc. (Tech.) degrees in electrical engineering from Aalto University, Espoo, Finland, in 2006 and 2019, respectively. He has been a Research Trainee with the Antennas and RF Technologies Team, VTT Technical Research Centre of Finland, Espoo, since 2005, where he has also been a Research Scientist since 2006. His current research interests include beam-steerable millimetre-wave antennas and arrays, integration, and packaging of RF components from microwave up to terahertz frequencies. He has over 40 publications in journals and conference proceedings. He is an active reviewer, for example, for IEEE Transactions on Antennas and Propagation, IEEE Antennas and Wireless Propagation Letters, and European Conference on Antennas and Propagation (EuCAP). He is a recipient of the 2017 EuMC Microwave Prize.

Jesús de Cos was born in Santander, Spain. He received the Telecommunications Engineering degree, the M.Sc. degree and the Ph.D. degree from the University of Cantabria, Santander, Spain, in 2010, 2011 and 2017, respectively. He joined ERZIA Technologies in 2016, where he is currently working in the design of RF and microwave systems. His research interests include the design and integration of microwave systems and circuit simulation techniques applied to microwave circuits. Dr. de Cos was awarded the Third Place Award for High Efficiency Power Amplifier Student Design in the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium Student Design Competition in 2016 and was a finalist in the IEEE MTT-S International Microwave Symposium Student Paper Competition in 2015.

Mario Giovanni Luigi Frecassetti received the degree in Electronics Engineering at the Politecnico di Milano in 1987. He is a veteran of wireless communications having started as Microwave designer in 1987 at Telettra that became Alcatel-Lucent and later NOKIA. He subsequently worked in the microwave system lab before joining the current position in the product strategy team. Currently he takes care, in addition to the product strategy activities of the Standardization & Regulation aspects in ETSI, ECC and ITU and the innovation activities in the field of mobile backhaul network. He leads, for NOKIA, the H2020 projects "DREAM" and “DRAGON” on D-Band (130-175GHz). He was awarded with the ALTA membership in 2005 and 2008, the Technical Career Track Principal Engineer in 2006 and rewarded by NOKIA Bell Labs with the Distinguished Member of technical Staff (DMTS) in 2012. He has authored or coauthored more than 15 patents and a lot of publications and white papers.

Maurizio Moretto Maurizio Moretto received the M.Sc. degree (laurea) in electronic engineering from Politecnico di Milano in 1988 with focus on digital signal processing. He started his career as a digital / DSP engineer for Telettra (later Alcatel) in the fields of automatic speech recognition and digital video compression. After a short experience in the Italian Army on artillery target tracking servo systems, he later joined Thales Alenia Space (formerly Laben) where he led the HW and DSP design team for spaceborne GPS / Glonass receivers for scientific applications. After moving to Ericsson, he continued his work on positioning as a technical coordinator of the GSM emergency call location service (E-OTD) development team, and took a new role as senior system engineer for the development of a high capacity QAM modem for point-to-point microwave fixed services. Maurizio Moretto is currently with Nokia X-Haul, working as a system engineer in close cooperation with the Nokia Bell Labs RFIC team on the development of millimeter-wave radio transceivers and phased arrays. He has authored and co-authored several papers in the fields of satellite communication systems, positioning and localization, RFICs for millimeter-wave communications.

Andrea Pallotta received the M.S. degree in electronic and telecommunication engineering from the University of Ancona, Italy, in 1990. After about one year period within the University of Ancona as a grant researcher, since 1991 to 1999 he has been with the Optoelectronic R&D Lab of Italtel, involved in many national and European projects as a senior designer. From 1998 to 2000 he was with the SDH Cross-Connect competence centre of Siemens as responsible of the Advanced Development Department. He joined ST end of 2000 as Design and Project Manager by leading the Optoelectronic and High Frequency Lab. His work has included the design and development of optoelectronic modules, GaAs MMIC, Bipolar, BiCMOS and BCD based silicon RFIC for high-speed data link, RF power amplifiers and RF transceivers. He is leading, since more than 20 years, both product development and coordination activities of several European R&D funded projects in the field of the optoelectronic and RF telecommunication systems. He is the author and co-author of 18 technical papers and holds 15 patents.

Vladimir Ermolov received the Ph.D in 1986 from the Moscow Engineering Physics University (MEPhI). Since 1986, he had been as Senior Research Associate with the laboratory of Dielectric Devices (MEPhI). He had been a principal research scientist with Nokia research center from1998 until 2011, where he worked as a project manager for many projects in areas of radio implementation, MEMS, nanotechnology, mass memory technology and sensors. Since 2011, he has been with VTT Technical Research Center of Finland at as a principal research scientist, where he had made project management and research in areas of millimeter wave communication, MEMS, nanotechnology, and technology commercialization. He is the author and co-author of 58 papers in referred journals and the holder and co-holder of 47 patents and patents pending. Vladimir Ermolov is a recipient of the 47th European Microwave Conference Microwave Prize.