Ultra-Low Phase Noise X-band BiCMOS VCOs Leveraging the Series Resonance

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***Abstract*— The most effective way to reduce phase noise in integrated harmonic oscillators is by rising the active power in the resonator i.e. scaling down the tank impedance and increasing power consumption. However, in widespread parallel-tank oscillators a lower bound is readily set by the smallest inductance that can be implemented without incurring into excessive degradation of the quality factor. Emerging multicore oscillators circumvent the issue only partially. In this paper, a circuit topology which breaks the phase noise barrier of parallel-tank oscillators is presented. By exploiting the same tank at the series resonance, the remarkably lower tank resistance allows to considerably rise the active power for given voltage swing. As a result, the phase noise is radically reduced without the need for aggressive scaling of the resonator inductor. Two VCOs in a BiCMOS 55nm technology exploiting the concept at 10GHz center frequency are presented. The first design targets an ultra-low phase noise and, with 9% tuning range, demonstrates -138dBc/Hz @ 1MHz offset with 1.2V supply and an excellent -190dBc/Hz FoM. The second design leverages a different implementation of the tank to expand the frequency tuning range and to trade phase noise for power consumption. The tuning range is 16% with minimum phase noise of -133 dBc/Hz@1MHz and -188dBc/Hz best FoM. To the Authors knowledge, the presented VCOs demonstrate experimentally the lowest phase noise ever reported with fully integrated oscillators in silicon technology.**

***Index Terms*—BiCMOS, millimeter wave, oscillator, phase noise, resonator, voltage-controlled oscillators.**

I. INTRODUCTION

Sustained by the deployment of the 5G network, an intense effort is ongoing toward development of silicon ICs for wireless communications at millimeter waves (mmWaves). In this context, research on high spectral purity oscillators attracts particular interest because the Local Oscillator (LO) phase noise is a major limiting factor to the wireless link performance [1] [2]. The LO phase noise gets intrinsically worst when the carrier frequency is raised into the mmWave band (either by designing oscillators at mmWaves or by using frequency multipliers) and the integrated phase noise bounds the modulation Error Vector Magnitude (EVM) [3] [4]. Therefore, development of ultra-low phase noise oscillators is crucial to enable high-capacity mmWave links with spectrally efficient modulation formats (e.g. M-QAM, with M>256) in the network infrastructure [5] [6].

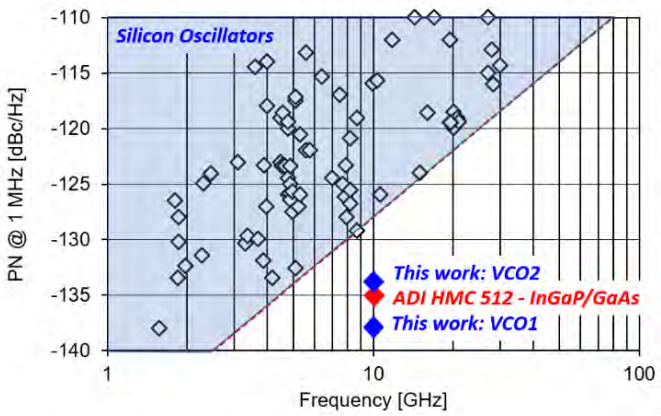

Fig. 1. Phase noise performance survey of VCOs in silicon technology and comparison with commercial products in III-V technology.

Integrated low-noise RF and mmWave oscillators consistently leverage an inductance-capacitance (L,C) tank at the parallel resonance. Although many different approaches have been investigated for improving the Figure of Merit (FoM) of oscillators [7] [8] [9] [10] [11], the phase noise can be substantially reduced, given the circuit topology and resonator quality factor, only by rising the active power on the tank [12]. But being the tank voltage swing bounded by the oscillator supply voltage, which is constrained by device reliability issues, the power on the resonator can be increased only scaling down the tank impedance (i.e. using a small inductance and a larger capacitance), and increasing the current consumption [13] [14]. However, Q degradation takes place with small inductors, penalizing the Figure of Merit (i.e. requiring higher power dissipation to meet the target phase noise) [15] and, with too small inductors, totally compromising the potential phase noise improvement. As a result, a lower bound exists on the minimum achievable oscillator phase noise in a given technology [16].

To scale down the phase noise further, oscillators evolved

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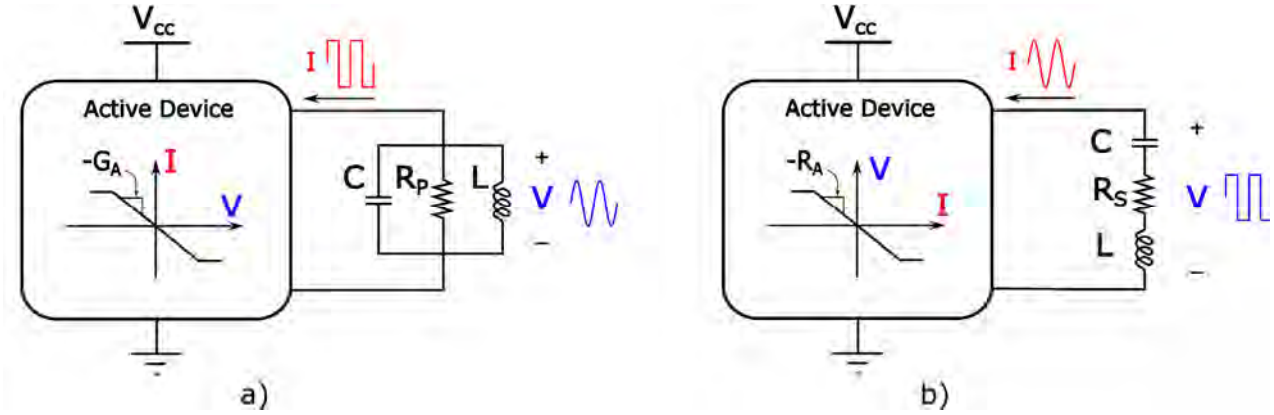

Fig. 2. Conceptual operation of a parallel-tank (a) and series-tank (b) oscillator.

from a single core to multi-core, where N oscillators are coupled and mutually synchronized to achieve a phase noise reduction of $10\log_{10}(N)$, compared to the single oscillator. The concept was explored by coupling two oscillators [17] [13] [18] [19] for 3dB phase noise scaling and extended to four [20] [21] [22] [23] [24] [14] [25] [26] [27] and up to eight [28] [29] [30] cores, leading ideally to 6dB and 9dB of phase noise reduction. On the other hand, multi-core oscillators bring several design concerns. Depending on the tank topology and coupling scheme, they may display unwanted multi-mode oscillations [24]. Moreover, when the number of cores is increased, very tight matching of the coupled oscillators is necessary to avoid phase noise penalty or even loss of synchronization [31] [22].

Despite the many efforts to improve spectral purity of voltage-controlled oscillators (VCO) in silicon, either with a single core or with the multi-core approach, the phase noise gap with VCOs in compound semiconductor technologies, which benefit from a remarkably higher supply voltage and higher quality factor of passive components, is still large.

Few works exploited resonators at the series resonance in oscillators for multi-phase generation [32] [33] [34]. In [35] it has been observed that this kind of oscillators have also the potential to achieve ultra-low phase noise without the need for aggressive scaling of the inductors. Nevertheless, the oscillator investigated in [35] looks relatively complex, consisting of a ring of four active stages interleaved by four series-tanks. Moreover, the potential phase noise advantage has not been demonstrated experimentally. This paper builds upon the observation in [35] and describes a novel oscillator topology suitable to drive an LC-tank at the series resonance to demonstrate an ultra-low phase noise [36]. Experimental results validate the concept and prove that this solution breaks the phase noise barrier of conventional parallel-tank oscillators. Two VCOs at 10GHz center frequency, implemented in a BiCMOS 55nm technology are presented. The first design targets an ultra-low phase noise and, with 9% tuning range, demonstrates -138dBc/Hz @ 1MHz offset with 1.2V supply and an excellent -190dBc/Hz FoM. The second design leverages a different implementation of the tank to expand the tuning range and to trade phase noise for power consumption. The tuning range is increased to 16% with minimum phase noise of -133 dBc/Hz@1MHz and -188dBc/Hz best FoM. Fig. 1 compares the VCOs performance against state of the art. The phase noise of the first design is at least 10dB lower than what reported so far in silicon. Moreover, the two oscillators match the performance of a commercial VCO in compound semiconductor technologies for test equipment's, telecom infrastructure and military applications [37].

The paper is organized as follows. Section II introduces and analyzes in detail the proposed oscillator circuit topology. A phase noise analysis is then proposed in Sect. IV while design of the test chips is described in Section V. Section VI presents experimental results and a more detailed comparison with state of the art. Finally, the conclusion follows in Section VII.

II. Series-Resonance Oscillator Concept

The phase noise advantage allowed by a tank operated at the series resonance is quantitatively evaluated in this section and then a circuit topology suitable to implement the active core of a series-tank oscillator is proposed.

Fig. 2 shows the conceptual block diagrams of oscillators with the LC-tank operated at the parallel and series resonance. In both cases, the phase noise due to white noise at offset $\Delta\omega$ from the (angular) oscillation frequency $\omega_0 = 1/\sqrt{LC}$ is given by [12]:

$$PN(\Delta\omega) = 10log_{10}\left(\frac{2Fk_BT}{P}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \qquad (1)$$

where k_B, T are the Boltzmann constant and absolute temperature, respectively, P is the active power dissipated on the resonator, with quality factor Q, and the noise factor F (>1) accounts for the extra noise added by the active core of the oscillator. Assuming the same noise factor for the active circuits in Fig. 2, from (1) the phase noise is only determined by the active power on the resonators, P. The equivalent resistance at the oscillation frequency of the parallel tank in Fig. 2a is $R_P = \omega_0 LQ$, while it is reduced to $R_S = \omega_0 L/Q = R_P/Q^2$ with the tank operated at the series resonance in Fig. 2b. Therefore, if the maximum voltage swing enforced by the active circuits across the two resonators is the same, the active power on the series tank is Q^2 times higher than that on the parallel tank, yielding, according to (1), a phase noise reduction of:

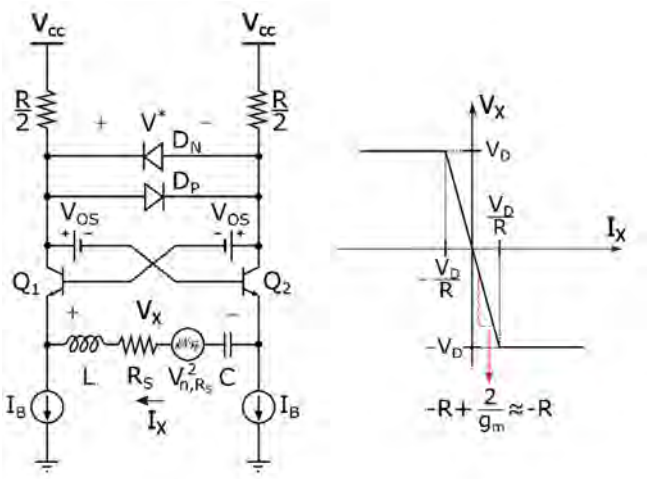

Fig. 3. Schematic of a series-resonance oscillator and static V-I characteristic of the active core.

$$PN_{series-tank} = PN_{parallel-tank} - 10log_{10}[Q^2] \quad (2)$$

The remarkable phase noise advantage obviously comes with the need for a correspondingly higher DC current consumption, required to reach the same voltage swing on the tank with a much lower resistance, but the oscillator power efficiency (or, equivalently, the FoM) is not necessarily penalized, being determined only by the active core circuit topology and by the tank Q factor [15]. On the opposite, for a low-phase noise design the series-tank oscillator maintains higher FoM because it does not need to scale down the inductor, as in the parallel-tank oscillator, to a value that compromises the Q factor.

To exploit the potential for ultra-low phase noise of the series resonator it is necessary to devise an active circuit suitable to drive it properly. The I-V curve at the port of the active core which shunts a parallel-tank must display the characteristic of a voltage-controlled negative resistor (VCNR). In a VCNR, the port current is a single-valued function of the port voltage [38]. On the other hand, if the tank is configured as a series resonator, the voltage across the tank must be a single-valued function of the current through the port of the active core, a condition achieved by implementing a current-controlled negative resistance (ICNR). The simplest and widely adopted VCNR in parallel-tank oscillators is the cross-coupled differential pair, with the static I-V characteristic illustrated in the box of Fig. 2a. At the quiescent point (V=0) the I-V curve shows a negative conductance ($-G_A$) while at large signal the current saturates to a maximum value. The series tank needs an ICNR circuit with the dual functionality, i.e. with the role of I and V exchanged. Shown inside the box in Fig. 2b, the V-I characteristic of the active core must provide negative resistance at the (unstable) equilibrium point ($-R_A$) and saturation of the voltage at large signal.

The schematic of the proposed circuit implementation is presented in Fig. 3. The series-tank (L, C, and the tank loss resistance Rs) is connected to the emitters of Q_1-Q_2, where the active core presents the static V_X-I_X characteristic drawn on the right side in Fig. 3. Looking at the circuit schematic, the

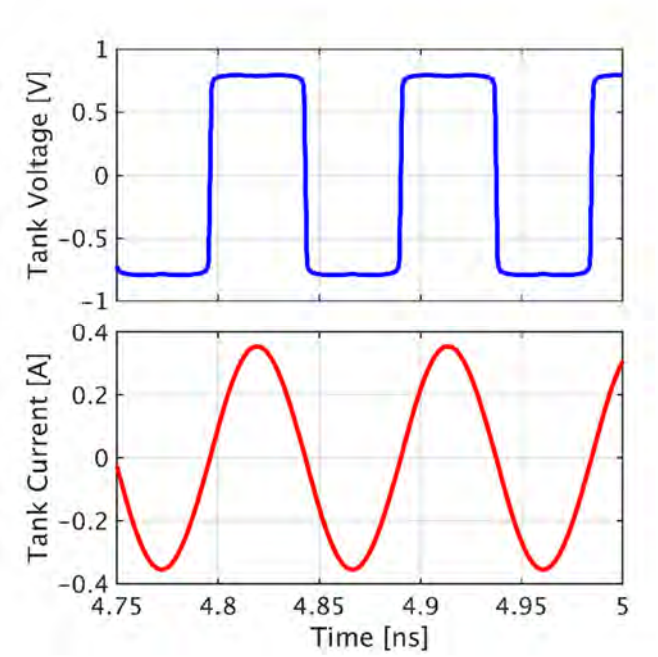

Fig. 4. Simulated tank voltage and current for the oscillator in Fig. 3.

batteries V_{os} represent a bias circuit which shifts down the base voltages of Q_1-Q_2 such that transistors remain in active region also at large signal. Q_1-Q_2 work as a differential emitter follower, forcing the voltage across the resonator, V_X, to be equal to -V*, the differential voltage at the collectors. At the equilibrium point (I_X=0), the same current flows through the load resistors R/2, V* is zero and the two diodes D_P-D_N are off. The positive feedback established by cross-coupling Q_1-Q_2 determines a negative resistance at the emitters nearly equal to the differential load resistance, $dV_X/dI_X \approx -R$. Oscillations built-up if $|R|>R_S$ [38]. When $|I_X|$ grows, the differential voltage drop on the load resistors rises, in magnitude, until one diode turns on (D_P if $I_X>0$, D_N if $I_X<0$) saturating V* and hence V_X to $\pm V_D$ (the diode voltage drop) when $|I_X| > V_D/R$. To gain insight on circuit operation, the oscillator is designed and simulated with a tank made of L_S=0.9nH, C_S=280fF and R_S=2.83Ω. The resonance frequency is 10GHz and the tank quality factor is Q=20. The load resistors are R/2=15Ω. The diodes $D_{N,P}$ and transistors $Q_{1,2}$, modeled with verilog-A code, are free of parasitic capacitors (modification to the circuit topology to accommodate device parasitic capacitors will be presented later in Sec. IV). Fig. 4 plots the resonator voltage and current in steady state from a transient simulation. The tank voltage looks like a square wave, with amplitude set by the diode's voltage drop, V_D~0.8V. On the other hand, the tank presents low impedance only at the fundamental frequency and the resonator current is therefore sinusoidal. The fundamental components of tank voltage and current can be approximated as:

$$V_0 = \frac{4}{\pi} V_D \quad (3)$$

$$I_0 = \frac{V_0}{R_S} = \frac{4}{\pi}\frac{V_D}{R_S} \quad (4)$$

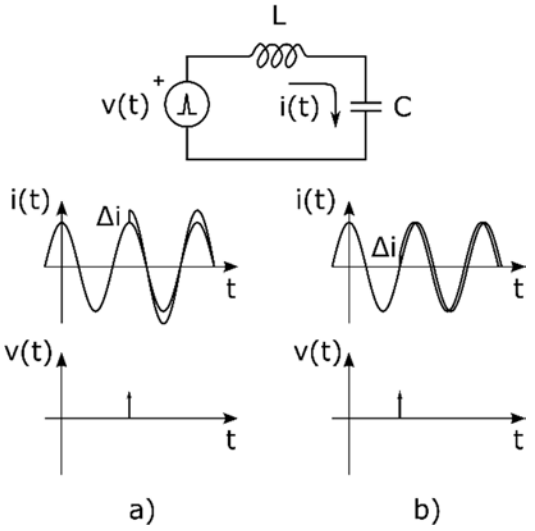

Fig. 5. Impulse sensitivity function test for a series-tank.

The current flowing through each transistor is $I_{Q1,2}(t)=I_B \pm I_{Tank}(t)= I_B \pm I_0 \sin(\omega_0 t)$ and, to avoid transistors turning-off during the oscillation cycle, the bias currents for the two branches of the circuit must be equal or larger than the peak current in the resonator given by (4), that is $I_B \geq I_0$.

III. Phase Noise Analysis

A rigorous phase noise analysis for the oscillator in Fig. 3 is presented in this section. For a generic harmonic oscillator, the phase noise is given by (1), with the impact of the different noise sources in the actual circuit implementation captured by *F*. Therefore, the purpose of the phase noise analysis is the evaluation of *F* for the circuit in Fig. 3. We can make use of the impulse sensitivity function (ISF) approach, widely adopted for the analysis of LC-tank oscillators [39] [40] [41] [42] [43]. The noise in parallel-tank oscillators is typically modeled as a current source in parallel with the tank, and the ISF measures the phase displacement generated by a current pulse at different time instants across one oscillation cycle [12]. In the dual case of a series-tank oscillator, it is more convenient to model the noise as a voltage source in series with the tank, as shown in Fig. 5. In this case, the ISF encodes the phase displacement generated by a voltage impulse at different time instants. As depicted in Fig. 5a, if the impulse is applied at the peak of the resonator current there will be only an amplitude change and no phase shift. On the other hand, if the impulse is applied at the zero crossing (Fig. 5b), it has maximum effect on the excess phase with almost no impact on the amplitude. Therefore, introducing $\theta = \omega_0 t$ and assuming a sinusoidal tank current, $I_{Tank} = I_0 \sin(\theta)$, the ISF associated to a noise voltage source in series with the tank is $\Gamma = \cos(\theta)$. Adapting the notation in [12] [42] to the case of a series resonator, and considering multiple noise sources, the oscillator phase noise can be expressed as:

$$PN(\Delta\omega) = 10log_{10}\left(\frac{\sum_i N_i}{2L^2 I_0^2 \Delta\omega^2}\right) \quad (5)$$

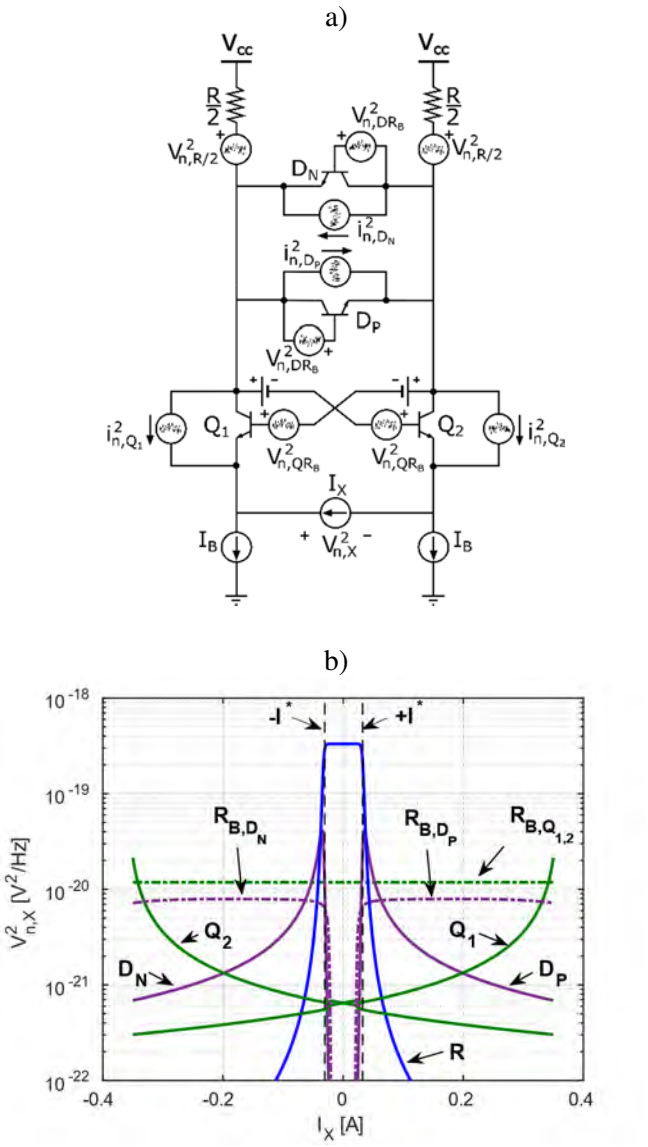

Fig. 6. Active core with the noise sources (a) and noise voltage PSDs across the port of the active circuit at different port current level (b).

with *L* the tank inductance and N_i (referred to as effective noise hereafter) given by

$$N_i = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(\theta) \cdot \overline{v_{n-i}^2}(\theta) d\theta \quad (6)$$

where $\overline{v_{n-i}^2}$ is the noise power spectral density (PSD) of the equivalent noise voltage source, in series with the tank, produced by the *i-th* device in the oscillator.

By observing that the active power on the resonator is $P = \frac{1}{2} R_S I_0^2$, and that the tank quality factor is $Q = (\omega_0 L)/R_S$, (5) can be recast to

$$PN(\Delta\omega) = 10log_{10}\left(\frac{\sum_i N_i}{R_S P}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \quad (7)$$

Now, by comparing (7) with (1), the noise factor is expressed in terms of effective noise contributions:

$$F = \frac{\sum_i N_i}{2k_B T R_S} \quad (8)$$

Shown in Fig. 3, the tank series resistance introduces thermal noise with a stationary PSD, $\overline{v_{n,Rs}^2} = 4k_B T R_S$ and the effective noise is immediately found with (6):

$$N_{R_S} = \frac{1}{2\pi}\int_0^{2\pi} cos^2(\theta) \cdot 4k_B T R_S \, d\theta = 2k_B T R_S \quad (9)$$

The situation is more complex for the noise sources in the active core, because the large-signal operation of transistors and diodes yields cyclo-stationary noise sources. Moreover, the two diodes D_N, D_P, turning on and off in each oscillation cycle, may change the transfer functions for some of the noise sources, leading to a cyclo-stationary PSD across the tank even for a stationary source. To gain insight, Fig. 6a shows the schematic of the active core with the noise sources considered in the analysis, and Fig. 6b plots the simulated noise voltage PSDs at the emitters of Q_1-Q_2, $\overline{v_{n,X}^2}$, sweeping the port current, I_X. Let's first consider the thermal noise contributed by the load resistors (the solid blue curve in Fig. 6b). As already anticipated, D_N and D_P are off when $|I_X| < I^* = V_D/R$. In this condition, the thermal noise of the two load resistors, $\overline{v_{n,R/2}^2}$=4kTR/2, is transferred by Q_1-Q_2 to the emitters, leading to a total noise PSD at the resonator port $\overline{v_{n,X}^2}\Big|_R$ = 2·4kTR/2. When I_X grows (in magnitude) and the diodes turn on, the resistors thermal noise circulates through the diodes and the noise at the output drops quickly. Therefore, we can approximate the thermal noise PSD contributed by the load resistors as:

$$\overline{v_{n,X}^2}\Big|_R \approx \begin{cases} 4k_B T R & if\ |I_x| < I^* \\ 0 & otherwise \end{cases} \quad (10)$$

When the resonator is connected to the active core, the port current corresponds to the tank current $I_{Tank} = I_0 \sin(\theta)$. Thus, the diodes are off near the zero crossings of the tank current i.e. for $|I_0 \sin(\theta)| < V_D/R$ or, equivalently, for $-\Phi < \theta < \Phi$ and $\pi-\Phi < \theta < \pi+\Phi$, with:

$$\Phi = \sin^{-1}\left(\frac{V_D}{RI_0}\right) \quad (11)$$

Noticing that the noise PSD given by (10) is nonzero only for $-\Phi<\theta<\Phi$ and $\pi-\Phi<\theta<\pi+\Phi$, the effective noise produced by the load resistors can now be computed again using (6):

$$N_R = \frac{1}{2\pi}\int_0^{2\pi} cos^2(\theta) \cdot \overline{v_{n,X}^2}\Big|_R \, d\theta = \frac{4k_B T R}{2\pi}\left[2\int_{-\Phi}^{\Phi} cos^2(\theta) d\theta\right] \quad (12)$$

An approximated closed form solution for the above integral is found assuming small Φ (i.e. $\cos(\theta)\approx 1$ in (12) and $\Phi \approx V_D/(RI_0)$ from (11)), a condition well verified in practice, leading to:

$$N_R \approx 2k_B T \frac{4}{\pi}\frac{V_D}{I_0} = 2k_B T R_S \quad (13)$$

where the last simplification is made by replacing I_0 with (4).

Going ahead with other noise sources, the PSD contributed by the extrinsic HBT base resistances is constant (dotted gray curve in Fig. 6b). The noise voltage of each resistor R_B, with PSD of $4k_BTR_B$, is transferred from the base of each HBT to the emitter, independently from the conduction state of D_N and D_P (ON or OFF) and this yields a stationary noise across the tank. Considering R_B noise for both Q_1 and Q_2, $\overline{v_{n,X}^2}\Big|_{R_{B-Q_{1,2}}} = 2\cdot 4k_BTR_B$ and the effective noise is readily calculated:

$$N_{R_{B-Q_{1,2}}} = \frac{1}{2\pi}\int_0^{2\pi} cos^2(\theta) \cdot 2 \cdot 4k_B T R_B \, d\theta = 4k_B T R_B \quad (14)$$

The solid green curves in Fig. 6b are the contribution to the output noise from the collector shot-noise current of Q_1-Q_2. The PSD of each noise current source, shown in the schematic of Fig. 6a, is $i^2_{n,Q1,2}=2k_BTg_{m1,2}$ ($g_{m1,2}$ is the transconductance of Q_1-Q_2). From circuit analysis, assuming high current gain of the transistors, the two noise current sources produce an output noise voltage with PSD $\overline{v_{n,X}^2}\Big|_{Q_{1-2}}$=$2k_BT/g_{m1}$+$2k_BT/g_{m2}$. Noticing that $g_{m1,2}=I_{C1,2}/V_T$ (with V_T the thermal voltage, $I_{C1}=I_B+I_x$, $I_{C2}=I_B-I_X$, the collector current of Q_1 and Q_2 respectively), and that when the active core drives the tank $I_x=I_{Tank}(\theta)$, using (6) the effective noise is:

$$N_{Q_{1,2}} = \frac{1}{2\pi}\int_0^{2\pi} cos^2(\theta) \cdot 2k_B T \left(\frac{V_T}{I_B + I_0 \sin\theta} + \frac{V_T}{I_B - I_0 \sin\theta}\right) d\theta \quad (15)$$

A closed form solution for (15) is found assuming the bias current is equal to the peak tank current, $I_B=I_0$, which is also the preferrable design choice to minimize the power consumption. In this case,

$$N_{Q_{1,2}} = 4k_B T \frac{V_T}{I_0} = 2k_B T R_S \frac{\pi}{2}\frac{V_T}{V_D} \quad (16)$$

with the right expression obtained by still replacing I_0 from (4).

If $D_{N,P}$ are implemented as diode-connected BJTs (i.e. with base and collector shorted), their primary noise contributions arise from the thermal noise of the base resistances and the collector current shot noise. Considering first the base resistances, (violet dotted curves in Fig. 6b), the thermal noise $4k_BTR_B$ appears at the emitters of $Q_{1,2}$ when one of the diodes turns on. Assuming an abrupt turn-on, the noise PSD can be approximated with

$$\overline{v_{n,X}^2}\Big|_{R_{B-D_{N,P}}} = \begin{cases} 4k_B T R_B & if\ |I_x| > I^* \\ 0 & otherwise \end{cases} \quad (17)$$

When the tank is connected to the active core, the port current is $I_{Tank} = I_0 \sin(\theta)$, D_P is on for $\Phi < \theta < \pi-\Phi$ while D_N is on for $\pi+\Phi < \theta < 2\pi-\Phi$. Applying (6), the effective noise is:

$$N_{R_{B-D_{N,P}}} = \frac{1}{2\pi}\int_0^{2\pi} cos^2(\theta) \cdot \overline{v_{n,X}^2}\Big|_{R_{B-D_{N,P}}} d\theta = \frac{4k_B T R_B}{2\pi}\left[2\int_{\Phi}^{\pi-\Phi} cos^2(\theta) d\theta\right] \approx 2k_B T R_B\left(1 - \frac{R_S}{R}\right) \quad (18)$$

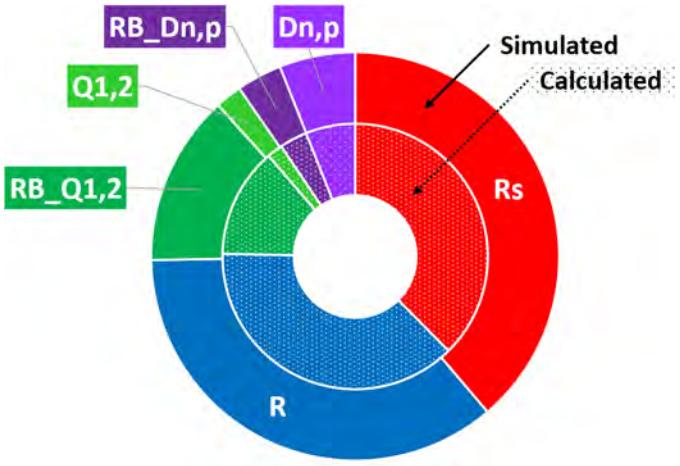

Fig. 7. Noise contribution: calculated versus simulated.

The last expression is achieved solving the integral assuming small Φ (i.e. approximating (11) with $\Phi \approx V_D/(RI_0)$) and replacing I_0 from (4). Last, the solid violet curves in Fig. 6b represent the noise PSD contributed by the shot noise of the diodes. Focusing on D_P, it turns on when $I_X > I^*$ and in this situation it can be modeled by an equivalent resistance, $r_{DP}=V_T/I_{DP}$ (I_{DP} being the diode current) with series voltage noise source with PSD $\overline{v_{n,D_P}^2} = 2k_BTr_{D_P}$, due to the collector shot noise. The output noise voltage due to the D_P shot noise is then equal to the noise PSD at the collectors of $Q_{1,2}$. Considering the voltage divider formed by r_{DP} and R/2, $\overline{v_{n,X}^2}\Big|_{D_P} = \left(R/(R+r_{D_P})\right)^2 \overline{v_{n,D_P}^2}$. Assuming abrupt turn-on of D_P, its current can be approximated as $I_{DP} = I_X - I^* = I_X - V_D/R$. When the active core drives the resonator, with current $I_{Tank}(\theta) = I_0\sin(\theta)$, D_P is on for $\Phi<\theta<\pi-\Phi$ with a current $I_{DP}=I_{Tank}(\theta) - V_D/R = I_0[\sin(\theta)-\sin(\Phi)]$. Being the situation is symmetrical for D_N, the effective noise produced by the shot noise of two diodes can be calculated with (6) as twice the effective noise of D_P:

$$N_{D_{N,P}} = 2\frac{1}{2\pi}\int_{\Phi}^{\pi-\Phi} cos^2(\theta)\cdot\left(\frac{R}{R+\frac{V_T}{I_0[\sin\theta-\sin\Phi]}}\right)^2 \cdot \cdot 2k_BT\frac{V_T}{I_0[\sin\theta-\sin\Phi]}d\theta \quad (19)$$

With some mathematical manipulations, and after replacing I_0 from (4), (19) can be well approximated by the following closed form expression:

$$N_{D_{N,P}} \approx k_BT\cdot R_S\frac{V_T}{V_D}\left[\ln\left(2\frac{V_D}{V_T}\frac{R}{R_S}+1\right)-1\right] \quad (20)$$

Finally, the noise factor is found replacing (9), (13), (14), (16), (18), (20) in (8):

$$F = \frac{N_{R_S}+N_R+N_{R_{B-Q_{1,2}}}+N_{Q_{1,2}}+N_{R_{B-D_{N,P}}}+N_{D_{N,P}}}{2k_BTR_S}$$

$$= 1+1+\frac{2R_B}{R_S}+\frac{\pi}{2}\frac{V_T}{V_D}+2k_BTR_B\left(1-\frac{R_S}{R}\right)+$$

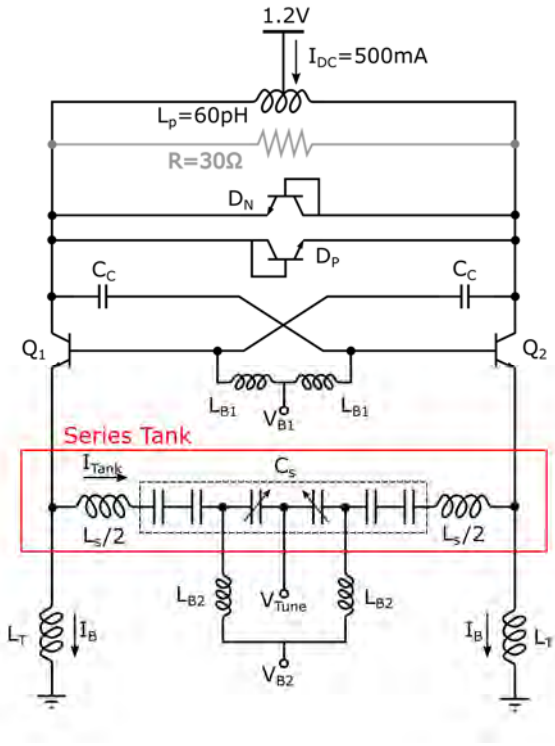

Fig. 8. Schematic of the implemented 10GHz series-resonance ultra-low phase noise VCO.

$$+\frac{1}{2}\frac{V_T}{V_D}\left[\ln\left(2\frac{V_D}{V_T}\frac{R}{R_S}+1\right)-1\right] \quad (21)$$

The phase noise analysis is finally validated against simulations, considering the oscillator design example introduced at the end of the Sec-II. The calculated total effective noise is $6.2\text{x}10^{-20}$ V^2/Hz, with the relative contributions of the different noise sources plotted in Fig. 7. The total effective noise from simulations is $6.05\text{x}10^{-20}V^2$/Hz, in good agreement with calculations. The simulated relative noise contributions, plotted in Fig. 7, are also in very good agreement with calculations. The noise factor, estimated with (21) is F=2.66, and the phase noise at 1MHz offset from the 10GHz oscillation frequency, calculated with (5), is -141dBc/Hz. Simulations predict F=2.58 and a phase noise of -141.1dBc/Hz.

IV. 10GHz Series-Resonance VCO Designs

Two series-resonance VCOs at 10GHz center frequency are designed in a BiCMOS 55nm technology. The first design targets the demonstration of an ultra-low phase noise, closing the gap between VCOs in silicon and in compound semiconductor technologies. In a second design, a different circuit implementation for the resonator is investigated to enhance the frequency tuning range and to trade phase noise for power saving.

A. VCO1: Design for ultra-low phase noise

The circuit schematic of the 10GHz VCO, designed to prove an extremely low phase noise, is shown in Fig. 8. Compared to the circuit introduced in Sec-II and shown in Fig. 3, few

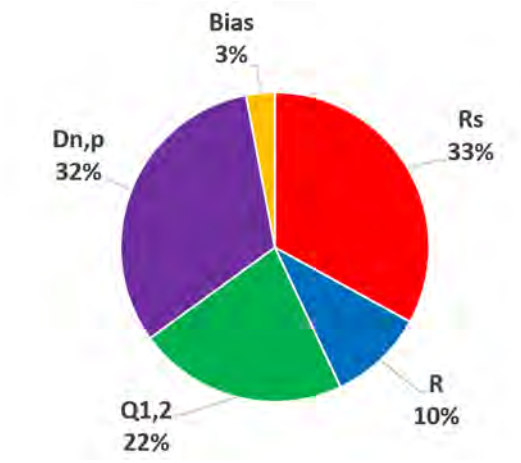

Fig. 9. VCO1 simulated noise contribution.

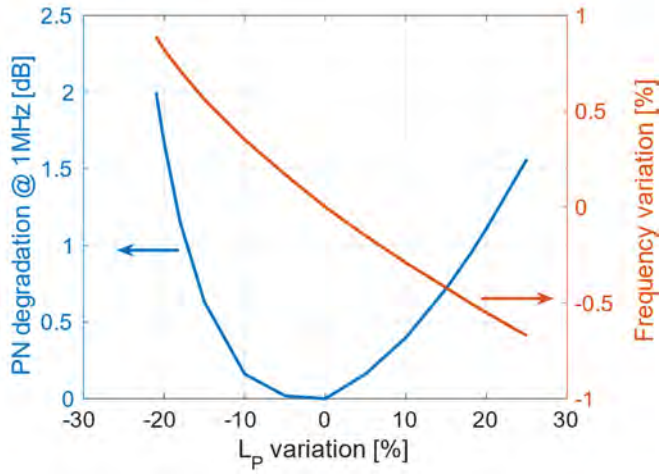

Fig. 10. Phase noise sensitivity to a variation of the load inductor L_P and influence on the oscillation frequency.

modifications are introduced. To avoid wasting voltage headroom and additional noise sources, the tail bias currents drawn in Fig. 3 are not implemented, while the DC currents for Q_1-Q_2 are sustained by the two inductors L_T[1]. The DC base voltage of Q_1-Q_2 is shifted down, with respect to the collectors, introducing the coupling capacitors (C_C) and by applying the bias voltage V_{B1} through the choke inductors, $L_{B1,}$ realized as multiturn spirals with a narrow-width trace. The bias voltage V_{B1} is generated by the diode of a current mirror (not shown), which sets the quiescent current with a 1:12 mirror ratio. Q_1-Q_2 are implemented as 36 parallel devices of 5x0.3μm^2. The total emitter-area is selected as a trade-off between parasitic caps and noise from the parasitic base resistance. The diodes D_N, D_P, limiting the voltage amplitude across the tank in steady-state, are realized with diode-connected HBTs[2]. A small and low-Q inductor L_P (~60pH) feeds the supply voltage to Q_1-Q_2 and resonates at 10GHz with the parasitic capacitances at the collectors of Q_1-Q_2. The equivalent resistance at the collectors (R, drawn in grey in Fig.8), required to have negative resistance across the main resonator, is due to the finite Q of L_P and of the choke inductors L_{B1}. The tank, connected at the emitters of Q_1-Q_2, is a series resonator tuned at 10GHz, with Q~20. The inductance, L_S~0.9nH, is realized as a single-turn spiral of 30μm trace width, symmetrically split in two parts, to host the tank capacitance in the center, C_S~280fF. The latter comprises two thick-oxide AMOS varactors in series with MOM capacitors. The tuning voltage is applied to the n-well of the varactors, while the gate terminals are biased at a constant voltage, V_{B2}=1.5V, through the compact choke inductors L_{B2} (sized such that the equivalent parallel resistance is sufficiently higher than the tank resistance at the series resonance). The differential voltage at the collectors of Q_1-Q_2, V*, is in good approximation a square wave with amplitude limited by D_N-D_P to V_D=0.8V. Due to the capacitive divider formed by C_C with the equivalent capacitance at the base of Q_1,Q_2, and the loading of the tank to the transistors, the voltage across the resonator follows V* but with some attenuation: $V_{tank}=\beta V^*$, where from simulations, β~0.75. The fundamental component of the voltage across the tank is relatively low, $V_0=(4/\pi)\beta V_D\approx 760$mV. However, the voltage on the series tank capacitor is boosted by Q-times, thus reaching a peak value slightly above 15V.

Therefore, to avoid reliability issues, the tank capacitance is implemented with the series of six capacitors (four MOM caps and two varactors). In this way the voltage on each component remains within the safe limits specified by the technology for long-term reliability. The peak current in the resonator is $I_0=V_0/R_S\approx 220$mA. Therefore, to avoid transistors turning off in the oscillation cycle, the nominal DC current in Q_1 and Q_2 is set by V_{B1} to 250mA. The supply voltage V_{CC} is chosen equal to the minimum required to keep the transistors operating in the active region, i.e. with $V_{CE}>V_{CEsat}\approx 0.4$V ($V_{CE\_sat}$ being the minimum collector-to-emitter voltage of the HBT to operate in the active region). The differential voltages at the collectors and at the emitters of Q_1-Q_2 are out of phase and with amplitude V_D and βV_D respectively. Considering the single-ended voltage amplitudes (i.e. half the differential one) the minimum supply is $V_{CCmin}=(1+\beta)V_D/2+V_{CEsat}=1.2$V.

The simulated phase noise at 1MHz offset from the 10GHz is -138dBc/Hz, 3dB higher than what simulated with the idealized circuit in Fig. 3. The primary reason is the decreased active power on the resonator due to the reduced tank voltage swing. The attenuation of the tank voltage by β=0.75 leads to a phase noise increase of $10\log(\beta^2)=2.5$dB. The other 0.5dB is due to a slight increase of the noise factor, from F=2.6 for the circuit in Fig. 3 to F=2.95 in the final design. This noise factor is nevertheless comparable or even lower than what achievable

[1] The two inductors L_T, in parallel with the main tank, also introduce a parallel resonance at lower frequency. But the ICNR characteristic of the negative resistance circuit ensures steady-state oscillation only at the series resonance.

[2] If the diodes are not used, the oscillation amplitude would be limited by the core HBTs (Q_1,Q_2) forced to enter the saturation region. In this situation, simulations point out a significant phase noise penalty, due to a larger contribution from the noise sources in Q_1,Q_2, including the noise of the forward-biased collector-base junctions.

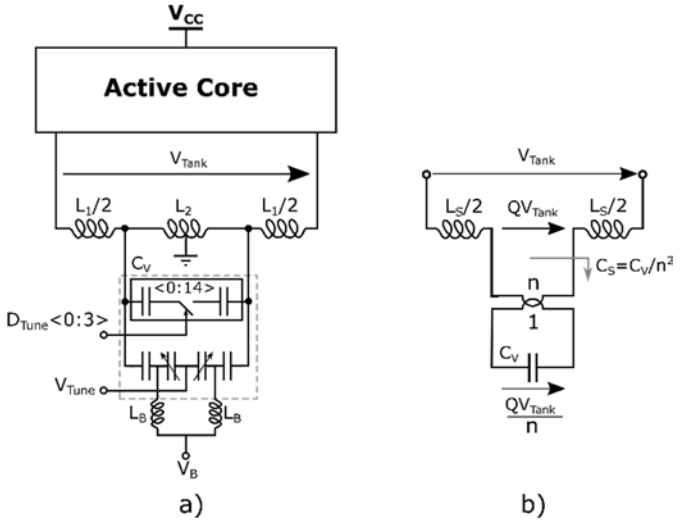

Fig. 11. Schematic of the tank with wide tuning range (a) and equivalent circuit near the series-resonance frequency (b).

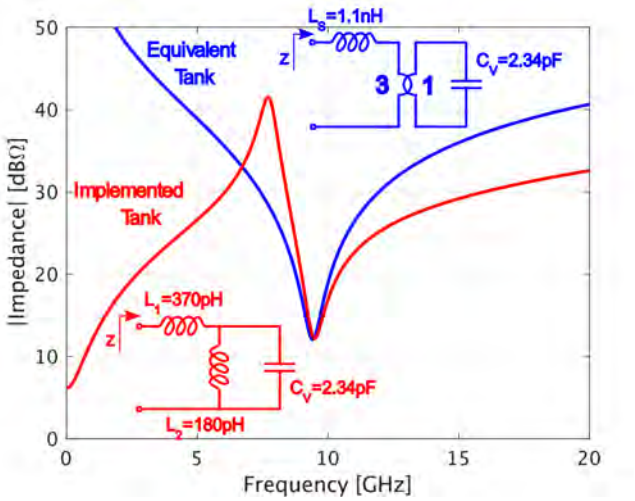

Fig. 12. Simulated impedance for the designed resonator and the equivalent circuit valid near the series-resonance frequency.

with parallel-tank oscillators, as it will be confirmed, in the next section, by comparing the measured oscillator FoM against previous works. Being the oscillator implemented with bipolar transistors, the $1/f^3$ phase noise corner is below 1kHz. The relative impact of the different noise sources at 1MHz offset is plotted in Fig. 9. Comparing Fig. 7 with Fig. 9, the tank noise contribution is reduced from ~38% to 33% while biasing components, not considered in the analysis, contribute 3% of the total. Interestingly, simulations on the implemented circuit point out also an increased contribution of the noise from Q_1-Q_2 and D_N-D_P which is almost completely balanced by a reduced impact of the thermal noise of the resistance R. The reduction of the noise contributed by R is attributed to the presence of the resonator at the collectors of $Q_{1,2}$, which prevents noise at the harmonics to be folded at the oscillation frequency. Meanwhile, the (parasitic) capacitances at the collectors of $Q_{1,2}$ sample the noise of $Q_{1,2}$ and $D_{N,P}$ when the diodes are ON, and inject this noise into the tank when the diodes turn OFF, near the zero-crossing of the current, i.e. at peaks of the ISF. As a result, the contribution of the core HBTs and diodes to phase noise is increased. A rigorous phase noise analysis to account for memory effects in the active core become way more complicated. However, despite the redistribution of the contributions in the active core, the analysis on the circuit in Fig. 3 predicts reasonably well both the noise factor and phase noise also for the implemented circuit.

Finally, the sensitivity of phase noise to a variation of the load inductor L_P has been checked with simulations. Although the impedance at the collectors of Q_1-Q_2 should be ideally resistive, a condition met only at the resonance frequency of L_P with the stray capacitances, simulations show that the oscillator is robust to variations of L_P (and hence of the impedance magnitude and phase at the collectors of $Q_{1,2}$). The phase noise degradation, plotted in Fig. 10, remains below 0.5dB and 1dB respectively for L_P within ±12% and ±18% from the optimal value. The oscillation frequency, reported in Fig. 10, is also mostly insensitive to L_P, being changed by only ±0.5% for L_P variation of ~±20%.

B. VCO2: Resonator modified for wider Tuning Range

The intrinsically high voltage on the capacitance of a series resonator, Q-times the voltage across the tank, poses a reliability issue due to the excessive voltage stress on the components. Adding fixed MOM capacitors in series to the varactors, as in the first proposed design, unavoidably limits the tank capacitance variation, finally penalizing the frequency tuning range. To solve the issue, a different solution for the resonator is investigated and implemented in a second design of the series-resonance VCO. Looking at Fig. 11a, the oscillator active core, inside the rectangular box, is the same as introduced in the first design, but the tank is now realized with an inductor, split in two parts (L_1,L_2), and a variable capacitor (C_V) directly connected across L_2. In this way, the tapped inductor works as a step-down transformer, reducing the voltage across L_2 such that fixed capacitors in series to the varactors (to limit the voltage stress) are no more required. Additionally, the grounded center tap of L_2 provides a DC current path for the oscillator core, avoiding the need for explicit DC-feed inductors (L_T in Fig. 8) and thus reducing silicon area occupation.

To gain further insight on the tank design, from network analysis the impedance seen across the two terminals of the resonator shows a parallel and a series resonance, at angular frequencies ω_P and ω_S respectively, given by:

$$\omega_P = \frac{1}{\sqrt{L_2 C_V}}, \quad \omega_S = \frac{1}{\sqrt{\frac{L_1 L_2}{L_1+L_2} C_V}} \qquad (22)$$

The ICNR characteristic of the active core guarantees that the oscillation builds-up at the series resonance [38] where the behavior of the network is the same of a simpler series tank, shown in Fig. 11b, formed by an equivalent inductance $L_{S\text{-}eq}$ and the capacitor C_V coupled with an ideal n:1 transformer. The

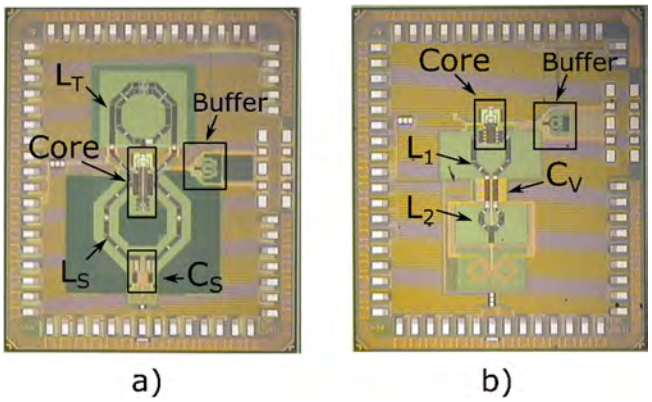

Fig. 13. Chip photo: VCO1 a), VCO2 b).

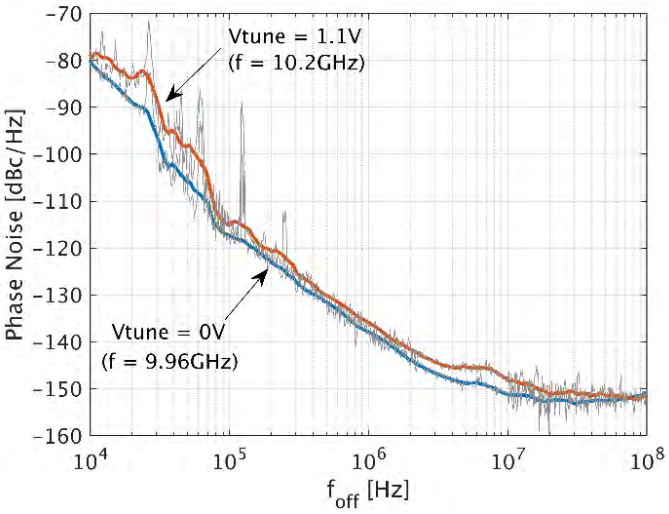

Fig. 14. Best and worst phase noise measured across the tuning range (VCO1).

transformer turns ratio, n, the equivalent inductance $L_{S\text{-}eq}$ and the quality factor of the equivalent resonator, Q_{eq}, are determined by L_1 and L_2, i.e. the position of the taps along the implemented inductor. From network analysis,

$$n = \frac{L_1+L_2}{L_2} \qquad (23)$$

$$L_{S-eq} = L_1 n = (L_1 + L_2)\,(n-1) \qquad (24)$$

$$Q_{eq} = \frac{Q_1 Q_2}{(1-n)Q_1 + nQ_2} \qquad (25)$$

with Q_1, Q_2 the quality factors of L_1, L_2.

Interestingly, if n>2 (a condition which is satisfied to scale the voltage on C_V down to a safe value) the equivalent resonator inductance $L_{S\text{-}eq}$ given by (24) is larger than the physical inductance (L_1+L_2). This feature may prove useful to design the oscillator with lower power consumption without requiring an excessively large inductance. In fact, if higher phase noise is acceptable, power consumption may be reduced implementing the tank with a larger inductance (and a smaller capacitance) to raise the equivalent tank resistance and, according to (1), reduce the active power on the resonator. However, with this design

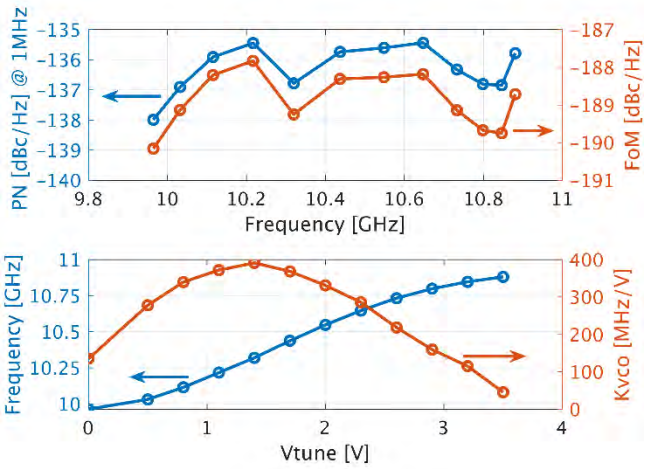

Fig. 15. Phase noise at a 1MHz offset and the FoM versus the oscillation frequency (top) and tuning characteristic (bottom) of VCO1.

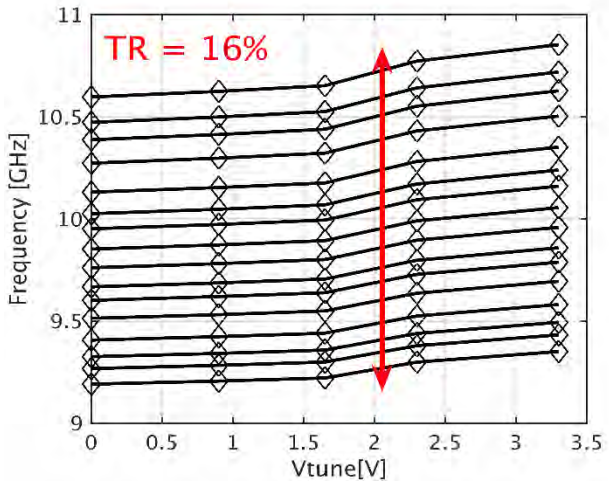

Fig. 16. Tuning characteristic of VCO2.

approach, silicon area increases. Moreover, the decrease of the self-resonance frequency sets an upper bound on maximum feasible inductor. The resonator in Fig. 11a displays an equivalent inductance at its series resonance which is larger than the physically implemented inductor, thus allowing to mitigate or circumvent the above issue. The resonator is designed with L_1=370pH and L_2=180pH giving, according to (23) and (24), n=3 and $L_{S\text{-}eq}$=1.1nH, twice the total implemented inductance of L_1+L_2=550pH. The variable capacitance C_V is realized with a bank of fifteen digitally switched MOM capacitors for coarse frequency tuning and a small varactor for fine tuning. At its maximum value, C_V=2.34pF, leading to a series resonance frequency calculated with (22) of $f_S = \omega_S/2\pi \approx$ 9.5GHz. The plot in Fig. 12 compares the simulated impedance of the implemented resonator (red curve) and the impedance of the equivalent circuit (blue curve) with components calculated with (23)(24)(25), proving a good agreement in the neighborhood of the series resonance.

The tank quality-factor, estimated with EM simulation on the implemented layout, is Q=17. The slightly lower Q, compared

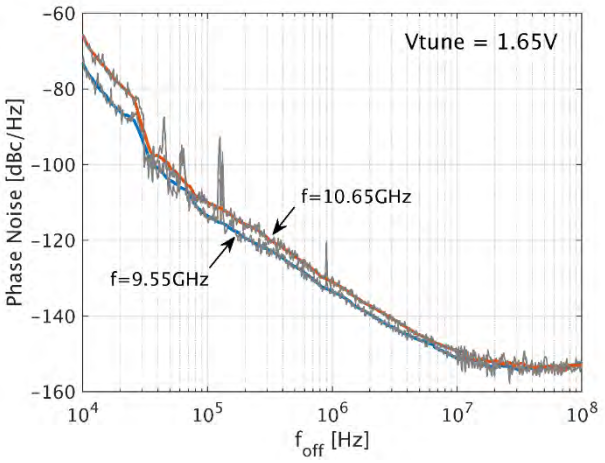

Fig. 17. Best and worst phase noise measured across the tuning range (VCO2).

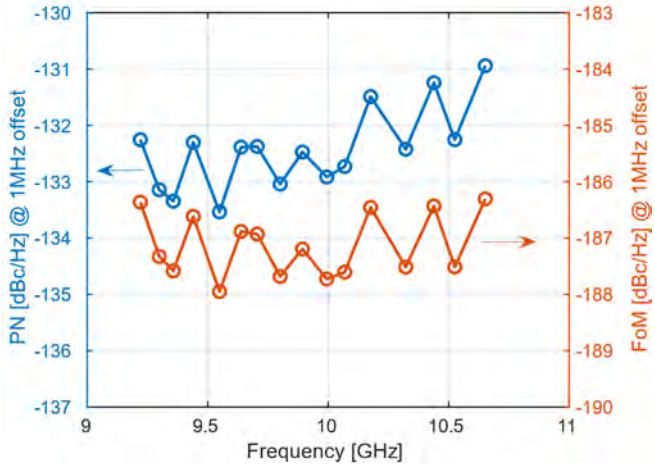

Fig. 18. Phase noise at a 1MHz offset and the FoM versus the oscillation frequency (VCO2).

to the tank in the first VCO, is due to the use of inductors of a smaller value and the resistance of long parallel traces used to connect the large tank capacitor. The tank equivalent resistance at the series resonance is 4.06Ω. The simulated fundamental component of the voltage across the tank is V_0≈760mV, as in the first designed VCO. With n=3 and Q=17 the maximum voltage across each capacitor is 2.1V, sufficiently low not to compromise the reliability. The simulated phase noise of the VCO is -133dBc/Hz@1MHz offset with a power consumption of 330mW from 1.2V supply.

V. Measurement Results

The two designed VCOs have been realized in the BiCMOS-55nm technology of STMicroelectronics and the chip photos are shown in Fig. 13. First, measurements on VCO1 are presented. Fig. 14 shows the phase noise versus the offset frequency from the carrier, measured with a spectrum analyzer, in the best and worst case across the frequency tuning range. The measurement at low offset frequency, up to nearly 100kHz, is likely impaired by random walk noise of the oscillator in free-run. The spurs visible in the measurement are likely due to a disturbance coupled through the supply or the test board, not sufficiently suppressed. At 1MHz offset, the best phase noise is -138dBc/Hz at 9.96GHz oscillation frequency. The worst phase noise is -135.5dBc/Hz at 10.2GHz oscillation frequency. The top plot in Fig. 15 shows the spot phase noise at 1MHz offset from the oscillation frequency and the VCO FoM across the tuning range. The power dissipation is 600mW from 1.2V supply and the FoM ranges from -190dBc/Hz to -188dBc/Hz. The bottom plot in Fig. 15 shows the tuning characteristic. Changing the varactor control voltage from 0V to 3.5V, the output frequency can be tuned from 9.96GHz to 10.9GHz, corresponding to 9% fractional tuning range. The peak tuning gain is Kvco=400MHz/V. The supply pushing, measured but not shown, is 53MHz/V.

VCO2 is tunable with a bank of digitally switched capacitors and a small varactor. Fig. 16 shows the tuning curves. The VCO tuning range is 16%, from 9.2GHz to 10.9GHz in 16 widely overlapped sub-bands. Fig. 17 shows the best and worst phase noise spectra across the digital tuning range when the varactor is biased in the middle of the control voltage (i.e. V_{tune}=1.65V). The best and worst measured phase noise at 1MHz offset are -133.5dBc/Hz and -131dBc/Hz at oscillation frequencies of 9.55GHz and 10.5GHz respectively. Fig. 18 plots the spot phase noise at 1MHz and the FoM across the tuning range. In VCO2 the DC power consumption is reduced to 330mW. The FoM ranges from -186.3dBc/Hz to -188dBc/Hz.

Finally, the performances of the two presented VCOs are summarized in Table I and compared against the best measurement results of other VCOs with oscillation frequency in the 10-20GHz range. The last but one column reports the calculated equivalent phase noise at 1MHz offset from 10GHz, such that a direct phase noise comparison is possible. To the Authors knowledge, the lowest phase noise in a silicon technology was demonstrated by [24], where a 4-core architecture in BiCMOS process achieved a minimum phase noise in the tuning range equivalent to -127.9dBc/Hz at 1MHz from 10GHz. The power consumption, from 3.3V supply, is 72mW giving a good FoM of -189dBc/Hz. The phase noise of a commercial product in III-V technology [37] is -135dBc/Hz, i.e. 7dB lower, although the power consumption (of more than 1W) is pretty high. The series-resonance VCOs close the phase noise performance gap, while maintaining high FoM. VCO1 displays a minimum phase noise 3dB below [37], and 10 dB lower than [24]. Notably, 10dB of phase noise scaling with the multi-core approach needs increasing the number of cores by more than 8 times (10Log(8)=9dB). This means, as an example, that the 4-core implementation in [24] would have to be extended to more than 32 cores, facing evident implementation issues. VCO2 proves the same tuning range of [24] with 5dB lower phase noise, still with a state-of-the-art FoM.

VI. Conclusion

In this paper, a novel harmonic oscillator circuit which drives a tank at the series resonance has been proposed. This solution

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

Reference	Tech.	N.Cores	V_{cc} [V]	P_{DC} [mW]	f_0 [GHz]	TR [%]	Area [mm^2]	Eq. PN (1MHz) @10GHz [dBc/Hz]	FoM [dBc/Hz]
[44]	130nm BiCMOS*	1	2	58	19.8	9.8	NA	-120.3	-181
[48]	130nm BiCMOS	1	3.3	122	20	18	0.087	-125.9	-185
[16]	55nm BiCMOS	1	2.5	56	20.5	19	0.045	-125	-187.5
[45]	130nm BiCMOS	1	4	70	21	20.5	0.069	-125.4	-187
[49]	120nm BiCMOS *	1	2.5	75	10.6	21.7	0.8***	-123.9	-184
[52]	250nm SiGe:C	1	3.7	93	12.8	5	0.25	-125.5	-185
[51]	130nm BiCMOS	1	3.3	45	17	15	0.065	-121	-184
[43]	130nm SiGe	1	3.4	65	12	10.6	NA	-125.6	-187
[22]	55nm BiCMOS*	4	1.2	50	20	15	0.6	-124.5	-187.5
[24]	130nm BiCMOS	4	3	72	15	16	1	-127.9	-189
[30]	28nm CMOS	8	1.1	173	10.7	27	3	-126.6	-184
[39]	GaAs InGaP HBT	NA	5	1650**	10	11.7	NA	-135	NA
This Work (VCO1)	**55nm BiCMOS**	**1**	**1.2**	**600**	**10**	**9**	**0.54**	**-138**	**-190**
This Work (VCO2)	**55nm BiCMOS**	**1**	**1.2**	**330**	**10**	**16**	**0.33**	**-134**	**-188**

* Only CMOS included in VCO core
** Including output buffer
*** Including pads

breaks the phase noise barrier of widespread oscillators based on parallel resonators. The remarkable phase noise advantage has been proved with a phase noise analysis and by experimental results on two VCOs, implemented in a BiCMOS process with 10GHz center frequency. The first VCO demonstrates a phase noise of -138dBc/Hz @ 1MHz offset, at least 10dB lower than what demonstrated in silicon technology so far. The second VCO exploits a different realization of the resonator to extend the frequency tuning range and to trade phase noise for power saving. The two VCOs match the performance of oscillators in compound semiconductor technologies for high-end applications.

As further research activity on this topic we recognize two important aspects: (1) a rigorous phase noise analysis in the finally implemented circuits can provide insights useful for phase noise optimization and FoM improvement, (2) feasibility in a pure CMOS technology, considering the potential issue arising from the high flicker noise, is certainly of high practical interest.

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