D-Band Antenna and Array Designs for 5G Applications

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***Abstract*— This paper presents the design, manufacturing and characterization of a parasitic patch microstrip D-band antenna and a 16-element segmented antenna array on a multilayer printed circuit board (PCB) targeted for 5G applications. The antennas are manufactured using printed circuit board technology with semi-additive processing (mSAP) of conductors on a multilayered substrate. The measured maximum gains for a single antenna and a 16-element array are respectively 9 dBi and 16.5 dBi at 157 GHz. The measured antenna array input matching bandwidth is 20 GHz.**

***Keywords*—antenna, antenna array, D-band, millimeter waves.**

I. Introduction

Thanks to the 31.8-GHz bandwidth allocated for wireless communications, the D-band (130–174.8 GHz) is being considered by industry as a very strong candidate for high capacity backhaul links for 5G and beyond [1]. The radio waves in D-band have low atmospheric attenuation but high free-space path losses. This promotes the importance of developing high gain D-band antennas. Especially, the development of D-band antenna arrays has raised interest. Utilization of a flat 2D phased-array antennas helps to overcome the free-space path losses with added capabilities such as self-alignment and pole-vibration mitigation via beam steering. D-band communication links with antenna arrays have been demonstrated in earlier works [2–4]. However, all demonstrators have very limited number of elements in antenna arrays. Up to 1024 elements in the antenna array are needed to obtain a practical gain for the D-band system [5]. Integration of RF modules with an antenna array has several challenges in the D-band. A common $\lambda_0/2$ distance between antenna elements is only 1 mm at 150 GHz. Thus, the physical dimensions of the antenna elements and their spacing become comparable to the size of the phased-array chipsets or even smaller [2]. Routing of interconnects needed for a case of 1024 antenna elements is extremely difficult. The efficiency of monolithic microwave integrated circuits (MMICs) is low in D-band and they generate plenty of heat. As the chip size also scales, the heat dissipation of a power amplifier can be as high as 1 W/mm^2 [2]. An architecture of a segmented antenna array is proposed as a compromise between a technical complexity and achievable performance of a D-band link [6]. In the architecture, a segmented antenna array is used in which several antenna elements are fed by a single phase-shifter and a power amplifier chain in a transmitter and several antenna elements are connected to a single LNA and phase-shifter chain in the receiver. Fig. 1 shows the architecture for the transmitter case.

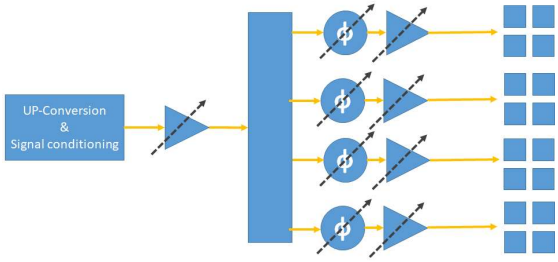

Fig. 1. Block diagram of a transmitter with a segmented antenna array (2×2 elements in each segment).

The main drawback of the proposed architecture is the generation of grating lobes due to the inability to control phasing of each individual antenna element. Thus, the effective element spacing is the spacing between the segments. However, because of the directive segment pattern, it was demonstrated that for steering a beam in a range of ±5°, grating lobes are 21 dB lower than the main lobe [6]. Such performance is sufficient for compensation of beam misalignments due to vibrations and displacements of the supports.

In the paper, we present a D-band parasitic patch microstrip antenna element designed for usage in the segmented antenna array. A 4×4 D-band antenna array utilizing the element is demonstrated also. The antenna is designed on a cost-effective and low-loss multilayer stack-up which is manufactured using advanced printed circuit board (PCB) processing technique. A semi-additive processing (SAP) is used. SAP allows fabrication of traces with a rectangular shape and limited deviation in its cross-section with the minimum required conductor width and spacing of 50 µm. This enables low RF transmission losses and reduced impedance variation.

II. PCB Stack Up and Antenna Design

A. PCB Stack Up

The PCB stack-up for the antenna test structures is shown in Fig. 2 from the chip level upwards. The stack-up is made of Panasonic Megtron7(N) (ε_r = 3.20, tanδ = 0.003 at 50 GHz) [7] dielectric material and copper layers. Glass-free resin coated

cu-foil (RCC) is used to meet needed design rules for the antenna stack-up and layer designs enabling thinner dielectric layers and smaller diameters of microvias. Stack-up dielectric and copper layer thicknesses are mostly 30 µm and 15 µm, respectively. The center core is 100 µm with 68 µm prepregs on both sides. For producibility, additional layers are needed above antenna elements for symmetry during fabrication. These layers are finally removed using 2.5D technology to provide a free space for radiation from the antenna. The PCB is manufactured as a high-density interconnection (HDI). It has laser-drilled microvias at stack-up layers which are plated through holes in the inner core. Landing pads with a minimum annular ring of 40µm are required for laser-drilling to compensate possible layer position inaccuracy. In addition, the PCB is thinned on the waveguide fixture probe area for a proper operation of the waveguide transition (seen in the lower sides in Fig. 4(e)–(f)). This waveguide transition is used for radiation pattern testing of the antenna prototypes. Details of the waveguide transition is described in [8]. The thinning and scoring of the transition antenna part is done by laser skiving.

B. *Antenna Element Design*

The parasitic patch microstrip antenna is selected as an antenna element for the segmented antenna array [9]. The antenna PCB build-up is shown in Fig. 2. The antenna is based on the aperture-coupled patch antenna with parasitic patches placed on top of a single driven patch to increase the antenna aperture size and thereby increase directivity and antenna gain. Such geometry allows to decrease losses in power dividers and feeding network required in a conventional 2×2 sub-array. A vertical microvia transition is included to feed the antenna from L7. A microstrip line on L17 is designed for the antenna test structures with probe pads or waveguide probe connection. The antenna is designed and optimized using the Ansys HFSS full wave EM simulator.

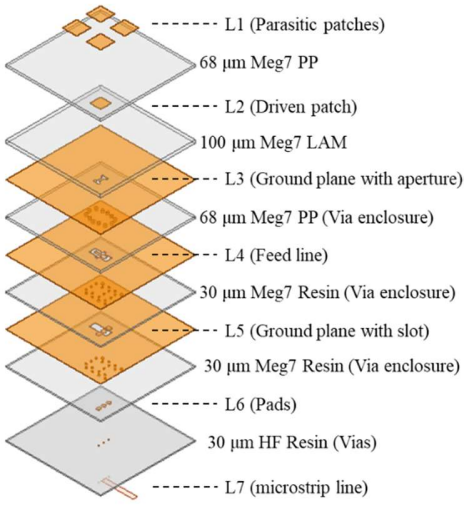

Fig. 2. PCB layer description and D-band antenna element design. "PP" denotes prepreg and "LAM" laminate.

Simulated reflection coefficients ($|S_{11}|$) for the antenna element are shown in Fig. 5. Simulated 2D gain pattern for the antenna is shown in Fig. 9 (a). The maximum gain of the antenna is 8.9 dBi.

C. *Antenna Array Design*

A 4×4 antenna array is also designed with an element spacing of 2 mm, i.e., λ_0 at 150 GHz. In addition, a feed network with microstrip line T-junctions on L17 is designed for the RF testing purposes. The array layout is presented in Fig. 3.

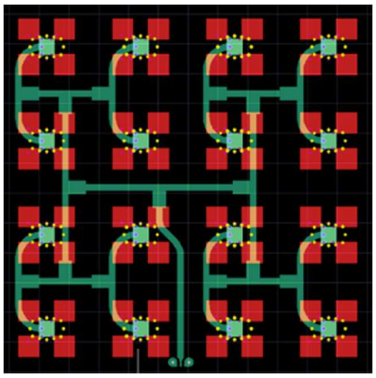

Fig. 3. Antenna array including the microstrip line feed network.

Simulated 2D radiation pattern of the 4×4 antenna array is shown in Fig. 9 (b). Simulations of the array are done using the single element pattern and so-called array-factor approach in the HFSS, i.e., feeding networks are not included. The maximum gain of the antenna array is 20.9 dBi.

III. Results and Discussion

The photographs of the manufactured antenna and array structures are shown in Fig. 5

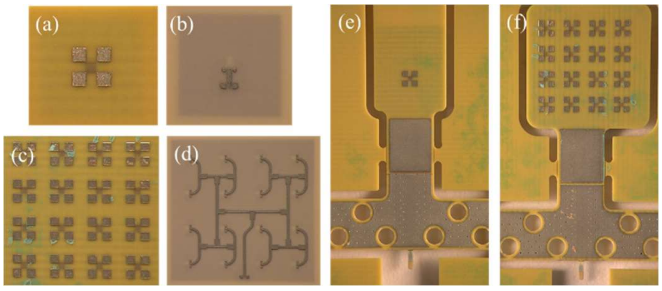

Fig. 4. Photographs of the antenna test structures. Single element with probe pads: (a) top side, (b) bottom side. Antenna array with probe pads: (c) top side, (d) bottom side. (e) Single element and (f) antenna array with waveguide interface.

A. *S-Parameters*

The S-parameters of the antenna element and the antenna array are measured at D-band (110–170 GHz) using PNA-X N5245A with WR6.5-VNAX extenders and GSG probes with 100-µm pitch. A Rohacell foam slab and an RF absorber were placed below the antenna-under-test (AUT) to emulate far-field radiation conditions.

Measured reflection coefficients ($|S_{11}|$) for antenna element and 4×4 array are shown in Fig. 5. The measured center

frequency is around 157 GHz whereas the simulated one is about 147 GHz. The difference could be due to small differences in the realized dimensions or substrate parameters. For the array, the measured center frequency is around 155 GHz. Input matching is better than for the single element due to insertion loss in the microstrip line feed network. The antenna impedance of the array is measured through 4 power divisions and lengthy feed lines.

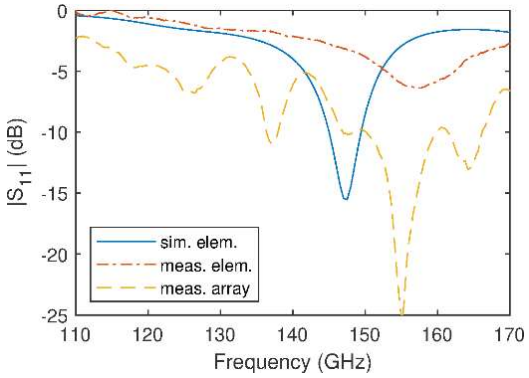

Fig. 5. Simulated and measured $|S_{11}|$ for single antenna and measured $|S_{11}|$ for antenna array.

The array feed network is simulated separately. Results for selected ports (port 1 as input, 2−5 as outputs) are presented in Figs. 6−7. Other array ports (6−17) are very similar due to symmetry. The simulated input matching $|S_{11}|$ is below -10 dB from 110 GHz up to 170 GHz (Fig. 6).

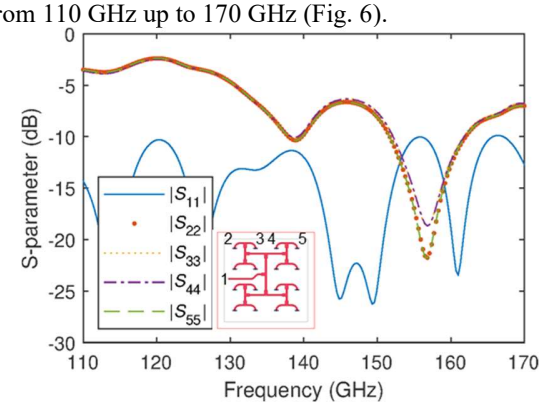

Fig. 6. Simulated reflection coefficients for selected ports of a 1-to-16 feed network. Port 1 is the input and other ones are outputs.

The output matchings ($|S_{22}|$…$|S_{55}|$) are below -6 dB above 132 GHz. The output matchings are worse than input matching due to inherent properties of the reactive quarter-wave matched T-junctions in the feed network. The transmission coefficients ($|S_{21}|$…$|S_{51}|$) from input to each output are displayed in Fig. 8. The insertion loss is about 16.5−18 dB at 150−160 GHz (Fig. 7). The additional losses in the microstrip lines of the feeding network are 4.5−6 dB in comparison with the ideal case (12 dB for the case of 4 dividers). The feed networks are designed for the antenna test structures only. In the final integration platform, the antennas are directly connected to the RF inputs/outputs of a vector modulator MMIC chip. The stand-alone feed network was not characterized due to lack of 50-Ω terminations for the array ports when measuring with a 2-port vector network analyser (VNA).

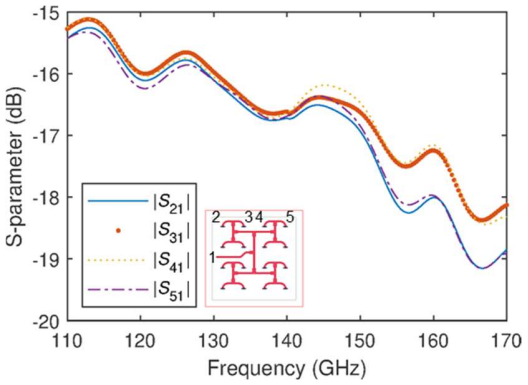

Fig. 7. Simulated transmission coefficients for selected ports of a 1-to-16 feed network.

B. Radiation Patterns

The radiation patterns of the antenna test structures were determined with the planar near-field measurement set up shown in Fig. 8. The setup is described with details in [9].

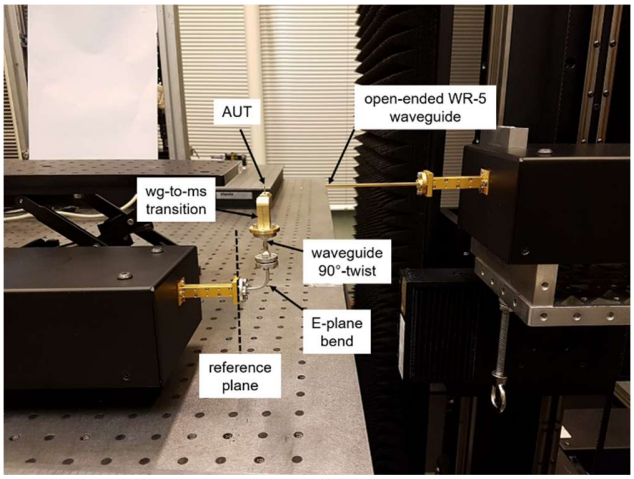

Fig. 8. Near-field measurement set-up. Open-ended WR-5 waveguide probe is attached to the VNA mm-wave extension, which is on the carriage of the planar near-field scanner. The probe is moved in the *xy*-plane to sample the near field. The absorbers are removed for clarity.

The measured 2D far-field plots for the antennas as a function of azimuth and elevation angles are presented in Fig. 9(c) and 9(d). The beam is wider for the single element than for the 4×4 antenna array. Some interference is observed in the single-element patterns presumably due to reflections, a leakage from the waveguide fixture, or truncation of the near-field scanning area. For the 4×4 array the main lobe is clearly visible and sidelobes can be seen in the angular range between

±70 deg. in the azimuth 0 deg. and elevation 0 deg. planes. The main beam and sidelobes, and beamwidths of the patterns are very similar to the simulated ones in Fig. 9(a) and 9(b).

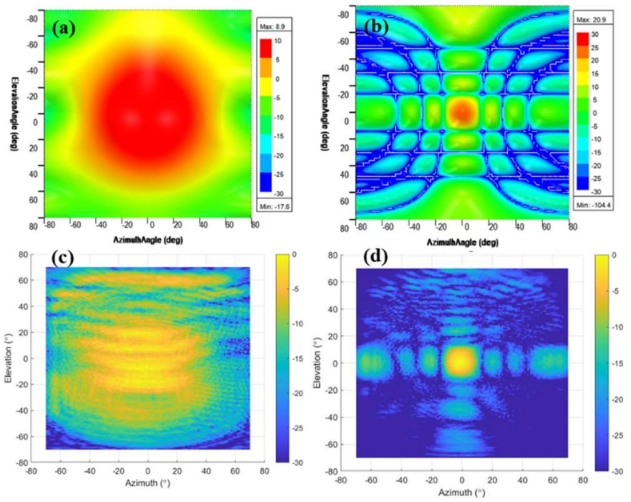

Fig. 9. Simulated radiation patterns for the (a) single element and (b) 4×4 antenna array (b). Measured radiation patterns for the (c) single element and (d) 4×4 antenna array.

The maximum gains as a function of frequency are presented in Fig. 10. For the single element the maximum gain is about 9 dBi around 157 GHz whereas for the array the maximum is 16.5 dBi. The simulated gain without feed network is 20.9 dBi, i.e., about 4.5 dB is lost due to the feed network. It is in line with the simulated feed network losses shown in Fig. 8.

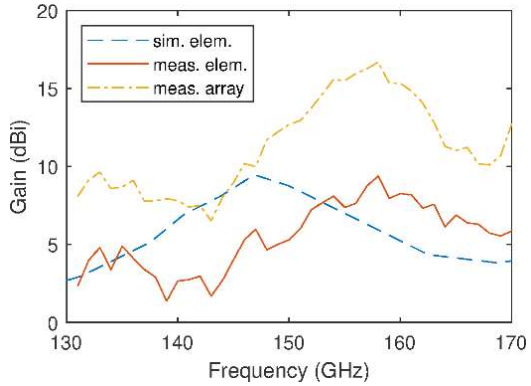

Fig. 10. Simulated and measured antenna gain for the single antenna and measured gain for the antenna array.

IV. Conclusion

Design, manufacturing, and characterization of a D-band parasitic microstrip antenna and a 4x4 antenna array on a multilayer high-frequency PCB is presented in the paper. The presented D-band antennas and PCB substrate technology show good performance and enable to be utilized in D-band link with a segmented phased antenna array.

Acknowledgment

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